Determining capacitor size and maximum sampling frequency for a nRF51 ADC voltage divider

The nRF51 ADC voltage divider model

The voltage divider circuit is as shown in figure 1.

![Voltage divider circuit for the nRF51 ADC](image)

<table>
<thead>
<tr>
<th>$t_{\text{SAMPLE}}$</th>
<th>8 bit resolution</th>
<th>20 $\mu$s</th>
</tr>
</thead>
<tbody>
<tr>
<td>$t_{\text{SAMPLE}}$</td>
<td>9 bit resolution</td>
<td>36 $\mu$s</td>
</tr>
<tr>
<td>$t_{\text{SAMPLE}}$</td>
<td>10 bit resolution</td>
<td>68 $\mu$s</td>
</tr>
<tr>
<td>$R_{\text{AIN}}$ 1/1 prescale</td>
<td></td>
<td>129.7 k$\Omega$</td>
</tr>
<tr>
<td>$R_{\text{AIN}}$ 2/3 prescale</td>
<td></td>
<td>194.6 k$\Omega$</td>
</tr>
<tr>
<td>$R_{\text{AIN}}$ 1/3 prescale</td>
<td></td>
<td>389.2 k$\Omega$</td>
</tr>
<tr>
<td>$U_{\text{ADC}}$ VBG reference</td>
<td></td>
<td>0.6 V</td>
</tr>
<tr>
<td>1 bit voltage for 8 bit resolution</td>
<td></td>
<td>4.71 mV</td>
</tr>
<tr>
<td>1 bit voltage for 9 bit resolution</td>
<td></td>
<td>2.35 mV</td>
</tr>
<tr>
<td>1 bit voltage for 10 bit resolution</td>
<td></td>
<td>1.17 mV</td>
</tr>
</tbody>
</table>

Table 1. nRF51 ADC values

Before ADC sampling, the capacitor $C$ will charge up since the input to the ADC is high impedance, i.e. $R_{\text{AIN}} = \infty$. When the ADC samples, $R_{\text{AIN}}$ will have value as shown in table 1. Duration of each sample is $t_{\text{SAMPLE}}$, also shown in table 1.

When sampling, current will flow from capacitor $C$ into the ADC through resistor $R_{\text{AIN}}$. The charge of the capacitor will hold $U_{\text{AIN}}$ steady during the sampling period, therefore eliminating the error caused by the high impedance voltage divider. The capacitor will of course discharge a little when sampling but the capacitor needs to be dimensioned so that the voltage error is less than what corresponds to 1 bit.
Deriving general equations

Steady state voltages for the circuit in Figure 1 are:

\[ U_{AIN,SS,\_sampling} = U_{BATT} \ast \frac{R_2 || R_{AIN}}{R_2 || R_{AIN} + R_1} + U_{ADC} \ast \frac{R_1 || R_2}{R_1 || R_2 + R_{AIN}} \]

\[ U_{AIN,SS,\_not\_sampling} = U_{BATT} \ast \frac{R_2}{R_1 + R_2} \]

where:

\[ R_1 || R_2 = \frac{R_1 \ast R_2}{R_1 + R_2} \]

The discharge voltage for the capacitor in Figure 1 is:

\[ U_{C, discharge} = U_0 (e^{-t/RC}) \]

Setting the discharge boundary equal to 1 bit voltage gives:

\[ U_0 - U_{1\_bit} = U_0 (e^{-t/RC}) \]

Isolating for C gives

\[ C = \frac{-t}{R \ln(U_0/U_{1\_bit})} \quad (equation \ 1) \]

where:

\[ U_0 = U_{AIN,SS,\_not\_sampling} - U_{AIN,SS,\_sampling} \]

\[ t = t_{SAMPLE} \]

\[ R = R_2 || R_{AIN} || R_1 \]

\[ U_{1\_bit} = 1 \text{ bit voltage} \]

Finding the maximum sampling frequency

Capacitor charging equation is

\[ U_{C, charge} = U_0 (1 - e^{-t/RC}) \]

The capacitor is estimated to be fully charged after 5*RC (99.3%). Maximum sampling frequency is therefore

\[ f_{max} = \frac{1}{5*RC} \]
where:
\[ R = R_2 || R_1 \]

**Calculation example**
For the example, following values are selected:
\[ U_{BATT} = 4.2 \text{V} \]
\[ R_1 = 10M\Omega \]
\[ R_2 = 2.2M\Omega \]
ADC prescaler: 1/1 \((R_{AIN} = 129.7k\Omega)\)
ADC resolution: 10 bit \(68\mu\text{s sampling period}\)

To find the capacitor value we insert the selected values into equation 1:

\[
U_{AIN,SS,sampling} = 4.2 \times \frac{2.2M||129.7k}{2.2M||129.7k+10M} + 0.6 \times \frac{10M||2.2M}{10M||2.2M+129.7k} = 0.0508 + 0.5597 = 0.6106 \text{V}
\]

\[
U_{AIN,SS,not,sampling} = 4.2 \times \frac{2.2M}{2.2M+10M} = 0.7574 \text{V}
\]

\[
U_0 = U_{AIN,SS,not,sampling} - U_{AIN,SS,sampling} = 0.7574 - 0.6106 = 0.1468 \text{V}
\]

\[
t = t_{SAMPLE} - 10 \text{ bit resolution} = 68 \mu\text{s}
\]

\[
R = R_2 || R_{AIN} || R_1 = \left( \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_{AIN}} \right)^{-1} = \left( \frac{1}{10M} + \frac{1}{2.2M} + \frac{1}{129.7k} \right)^{-1} = 121.0 \text{k}\Omega
\]

\[
U_{1bit} = 1 \text{ bit voltage for 10 bit resolution} = 1.17 \text{ mV}
\]

\[
C = \frac{-68\mu}{121.0k \times \text{ln}\left(\frac{146.8m}{146.8m-1.17m}\right)} = 70.3 \text{ nF}
\]

The maximum sampling frequency for this setup is:

\[
f_{max} = \frac{1}{5 \times RC} = \frac{1}{5 \times R_2 || R_1 \times C} = \frac{1}{5 \times 1.803M \times 70.3n} = 1.58 \text{ Hz}
\]