Determing capacitor size and maximum sampling frequency for a nRF51 ADC voltage divider

The nRF51 ADC voltage divider model

The voltage divider circuit is as shown in figure 1.

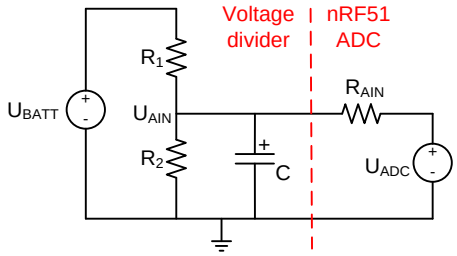

Figure 1. Voltage divider circuit for the nRF51 ADC

t_{SAMPLE} – 8 bit resolution	20 μs
t_{SAMPLE} – 9 bit resolution	36 μs
t_{SAMPLE} – 10 bit resolution	68 μs
R_{AIN} – 1/1 prescale	129.7 kΩ
R_{AIN} – 2/3 prescale	194.6 kΩ
R_{AIN} – 1/3 prescale	389.2 kΩ
U_{ADC} – VBG reference	0.6 V
1 bit voltage for 8 bit resolution	4.71 mV
1 bit voltage for 9 bit resolution	2.35 mV
1 bit voltage for 10 bit resolution	1.17 mV

Table 1. nRF51 ADC values

Before ADC sampling, the capacitor C will charge up since the input to the ADC is high impedance, i.e. $R_{AIN} = \infty$. When the ADC samples, R_{AIN} will have value as shown in table 1. Duration of each sample is t_{SAMPLE}, also shown in table 1.

When sampling, current will flow from capacitor C into the ADC through resistor R_{AIN}. The charge of the capacitor will hold U_{AIN} steady during the sampling period, therefore eliminating the error caused by the high impedance voltage divider. The capacitor will of course discharge a little when sampling but the capacitor needs to be dimensioned so that the voltage error is less than what corresponds to 1 bit.

Deriving general equations

Steady state voltages for the circuit in Figure 1 are:

$$U_{AIN\_SS\_sampling} = U_{BATT} * \frac{R_2||R_{AIN}}{R_2||R_{AIN}+R_1} + U_{ADC} * \frac{R_1||R_2}{R_1||R_2+R_{AIN}}$$

$$U_{AIN\_SS\_not\_sampling} = U_{BATT} * \frac{R_2}{R_1+R_2}$$

where:
$R_1||R_2 = \frac{R_1*R_2}{R_1+R_2}$

The discharge voltage for the capacitor in Figure 1 is:
$U_{C\_discharge} = U_0(e^{-t/RC})$

Setting the discharge boundary equal to 1 bit voltage gives:

$$U_0 - U_{1bit} = U_0(e^{-t/RC})$$

Isolating for C gives

$$C = \frac{-t}{R*\ln(\frac{U_0-U_{1bit}}{U_0})} \quad (equation\ 1)$$

where:
$U_0 = U_{AIN\_SS\_not\_sampling} - U_{AIN\_SS\_sampling}$
t = t_{SAMPLE}
R = $R_2||R_{AIN}||R_1$
U_{1bit} = 1 bit voltage

Finding the maximum sampling frequency

Capacitor charging equation is

$$U_{C\_charge} = U_0(1 - e^{-t/RC})$$

The capacitor is estimated to be fully charged after 5*RC (99.3%). Maximum sampling frequency is therefore $f_{max} = \frac{1}{5*RC}$

where:
R = $R_2||R_1$

Calculation example

For the example, following values are selected:
U_{BATT} = 4.2V
R_1 = 10MΩ
R_2 = 2.2MΩ
ADC prescaler: 1/1 (R_{AIN} = 129.7kΩ)
ADC resolution: 10 bit (68µs sampling period)

To find the capacitor value we insert the selected values into equation 1:

$U_{AIN\_SS\_sampling}$ = 4.2 * $\frac{2.2M||129.7k}{2.2M||129.7k+10M}$ + 0.6 * $\frac{10M||2.2M}{10M||2.2M+129.7k}$ = 0.0508 + 0.5597 = 0.6106 V
$U_{AIN\_SS\_not\_sampling}$ = 4.2 * $\frac{2.2M}{2.2M+10M}$ = 0.7574 V
$U_0 = U_{AIN\_SS\_not\_sampling} - U_{AIN\_SS\_sampling}$ = 0.7574 – 0.6106 = 0.1468 V
t = t_{SAMPLE} – 10 bit resolution = 68 μs
R = $R_2||R_{AIN}||R_1 = (\frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_{AIN}})^{-1} = (\frac{1}{10M} + \frac{1}{2.2M} + \frac{1}{129.7k})^{-1}$ = 121.0 kΩ
U_{1bit} = 1 bit voltage for 10 bit resolution = 1.17 mV

C = $\frac{-68\mu}{121.0k*\ln(\frac{146.8m-1.17m}{146.8m})}$ = 70.3 nF

The maximum sampling frequency for this setup is:

$f_{max} = \frac{1}{5*RC} = \frac{1}{5*R_2||R_1*C} = \frac{1}{5*1.803M*70.3n}$ = 1.58 Hz