QM13345

SP4T (Single-Pole-Four-Throw Switch)

Product Description

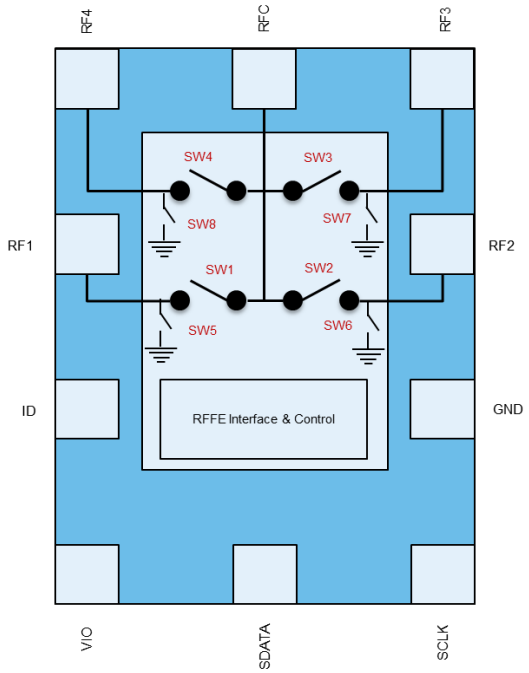
The QM13345 is specifically designed for wideband and high-performance tuning applications. With ultra-low RON and low COFF coupled with selectable OFF ports to eliminate parasitic resonances enables creation of advanced tuning architectures to maximize TRP & TIS.

10 Pin 1.1 x 1.5 x 0.44 mm Module Package

Feature Overview

- Very Good Performance
  - Ultra-Low R_{ON}: 0.8Ω
  - Very Low C_{OFF}: 145fF
- High RF voltage handling capability: >55Vp
- RFFE 2.1 Control Interface
- Requiring only a single supply – VIO (No VDD)
- Off Ports, 'OPEN Type' or 'GROUND Type'
- 3 Selectable USID using external pin, ID
- Very Small 1.1mm x 1.5mm, module package
- Suitable for all cellular applications including 5G with broadband performance up to 7.2GHz

Functional Block Diagram



Top View

Applications

- Antenna Tuning
- Band Switching
- Impedance Tuning

Ordering Information

PART NO.	DESCRIPTION
QM13345SB	5-pc Sample Bag
QM13345SR	100-pc, 7" Reel
QM13345TR13	10000-pc, 13" Reel
QM13345DK	Design Kit
QM13345EVB	Evaluation Board

Absolute Maximum Ratings

PARAMETER	RATING
Storage Temperature	-40 to 150 °C
Operating Temperature	-30 to 90 °C
V_{IO},SDATA, SCLK	2.5V
Max RF Voltage between RFC port and Ground (V_{RF}) V_{IO}=1.8V, Temp=25 °C	55V_P

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS: Nominal conditions are unless otherwise specified. V_{IO} = 1.8V, Temp = 25ºC, 50 Ω, Active Mode.
V_{IO} - Interface Supply Voltage	1.65	1.8	1.95	V	
I_{VIO} - Interface Supply Current		40		µA	Active Mode
		2		µA	Low Power Mode
ID, SDATA, SCLK - Control Voltage High	0.8*V_{IO}	V_{IO}	1.95	V	Must not exceed V_{IO} voltage

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, off ports closed, Input and Output = 50Ω, T = 25°C, V_{IO} = 1.8V, SDATA/SCLK = 1.8 V / 0 V

PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Insertion Loss RFC to RF1, RF2, RF3, RF4 Single Switch Path ON	600 – 960 MHz		0.17		dB
	1710 – 2170 MHz		0.29		dB
	2170 – 2690 MHz		0.38		dB
	3300 – 4200 MHz		0.97		dB
	4200 – 5000 MHz		1.7		dB
	5000 – 6000 MHz		2.6		dB
	6000 – 7125 MHz		3.7		dB
Isolation RFC to RF1, RF2, RF3, RF4 Single Switch Path ON	600 – 960 MHz		39		dB
	1710 – 2170 MHz		28		dB
	2170 – 2690 MHz		24		dB
	3300 – 4200 MHz		18		dB
	4200 – 5000 MHz		15		dB
	5000 – 6000 MHz		13		dB
	6000 – 7125 MHz		12		dB
R_{ON}	ON – State		0.8		Ω
C_{OFF}	RFC to RF1 & RFC to RF2 – All Switches Off		145		fF
	RFC to RF3 & RFC to RF4 – All Switches Off		160		fF
Second Harmonic	fo = 700MHz; Pin = 23dBm		-95		dBm
Third Harmonic			-100		dBm
Second Harmonic	fo = 915MHz; Pin = 35dBm		-74		dBm
Third Harmonic			-62		dBm
Second Harmonic	fo = 1910MHz; Pin = 33dBm		-67		dBm
Third Harmonic			-62		dBm
Second Harmonic	fo = 2570MHz; Pin = 23dBm		-82		dBm
Third Harmonic			-90		dBm
ON Switching Time	End of Register Write to 90% final RF Amplitude		6		µs
OFF Switching Time	End of Register Write to 10% final RF Amplitude		6		µs
IIP2	Refer to IIP2 conditions table		134		dBm
IIP3	Refer to IIP3 conditions table		76		dBm

IIP2 Test Conditions

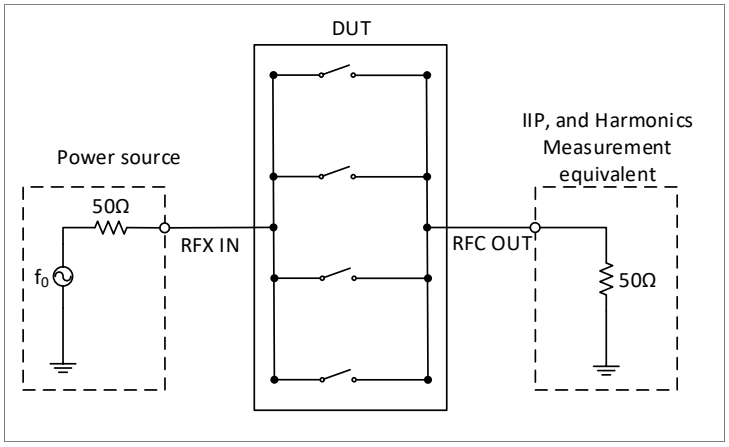
Band	In-Band freq	CW tone 1		CW tone 2	
	[MHz]	[MHz]	[dBm]	[MHz]	[dBm]
Band I Low (IMT)	2140	1950	+20	190	-15
Band I High (IMT)	2140	1950	+26	4090	-20
Band V Low (Cell)	881.5	836.5	+20	45	-15
Band V High (Cell)	881.5	836.5	+26	1718	-20

IIP3 Test Conditions

Band	In-Band freq	CW tone 1		CW tone 2	
	[MHz]	[MHz]	[dBm]	[MHz]	[dBm]
Band V High (Cell)	881.5	836.5	+20	791.5	-15
Band I High (IMT)	2140	1950	+20	1760	-15

Test Setup

IIP2, IIP3 and Harmonic Measurement Setup



Power Modes and Triggering & USID_SEL Pin Connection

As per RFFE specification, register 28 is used for setting the power mode of the device and triggering functionality.

- Active Mode – Set register 28 bits D7:D6 to 00. REG_07<7:0>=00XXXXXX
- Low Power Mode – Set register 28 bits D7:D6 to 10. REG_07<7:0>=10XXXXXX

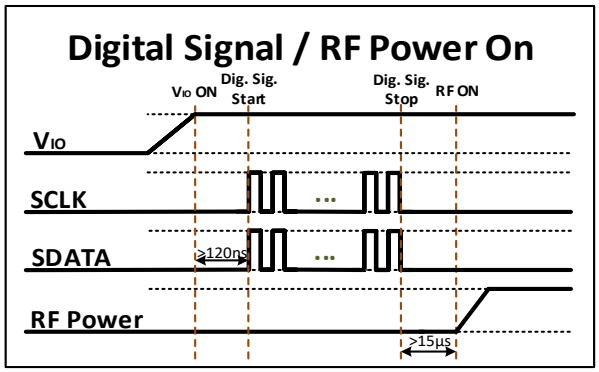
An external pin, ID, on the QM13345 provides the user with an option to set up to 3 of the USID. The ID pin can be used to set the USID to either 0110, 0111 or 0100. The ID pin can be connected to GND, VIO, or float.

ID PIN CONNECTION	USID [S3:S0]
Connect to V_{IO}	0110
Connect to GND	0111
float	0100

Timing Requirements

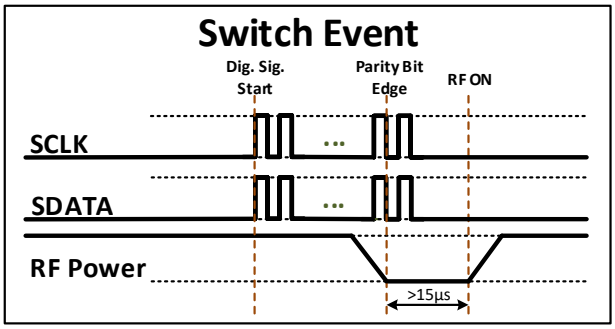
It is very important that the user adheres to the correct timing sequences in order to avoid damaging the device. Figures are NOT drawn to scale.

1. VIO must be applied for a minimum of 120 ns before sending SDATA/SCLK to ensure correct data transmission.
2. Wait a minimum of 15µs after RFFE bus is idle to apply an RF signal.



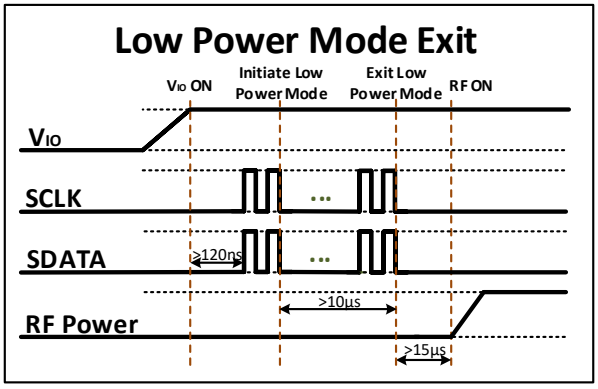
Digital Signal / RF Power-On Detail

3. RF power must not be applied during switching events. To ensure this, remove RF power before completing a register write that will change the switch mode.



Switch Event Timing

4. If “Low Power Mode” is utilized, there must be a delay of 10 µs before exiting “Low Power Mode”.



Low-Power Mode Exit Timing

Control Logic Table

Register 0x00 and Register 0x01 control each of the 4 series and 4 shunt switches of the device. Each switch is controlled by an individual bit within the register. If a bit is low, the corresponding switch will be OFF, and if a bit is high, the corresponding switch will be ON. Multiple switches may be turned on simultaneously.

NOTE: Register 0x00 and Register 0x01 are OR'd together. If Reg 0x00 is used, do not write to Reg 0x01, and vice versa.

Register 0x00/0x01									
Bits 7:4 – Shunt SW Control				Bits 3:0 – Series SW Control					
B7	B6	B5	B4	B3	B2	B1	B0	Shunt Switch ON	Series Switch ON
0	0	0	0	0	0	0	0	All Off	All Off
0	0	0	0	0	0	0	1	All Off	RF1
0	0	0	0	0	0	1	0	All Off	RF2
0	0	0	0	0	0	1	1	All Off	RF2, RF1
0	0	0	0	0	1	0	0	All Off	RF3
0	0	0	0	0	1	0	1	All Off	RF3, RF1
0	0	0	0	0	1	1	0	All Off	RF3, RF2
0	0	0	0	0	1	1	1	All Off	RF3, RF2, RF1
0	0	0	0	1	0	0	0	All Off	RF4
0	0	0	0	1	0	0	1	All Off	RF4, RF1
0	0	0	0	1	0	1	0	All Off	RF4, RF2
0	0	0	0	1	0	1	1	All Off	RF4, RF2, RF1
0	0	0	0	1	1	0	0	All Off	RF4, RF3
0	0	0	0	1	1	0	1	All Off	RF4, RF3, RF1
0	0	0	0	1	1	1	0	All Off	RF4, RF3, RF2
0	0	0	0	1	1	1	1	All Off	RF4, RF3, RF2, RF1

Register 0x00/0x01									
Bits 7:4 – Shunt SW Control				Bits 3:0 – Series SW Control					
B7	B6	B5	B4	B3	B2	B1	B0	Shunt Switch ON	Series Switch ON
1	1	1	1	0	0	0	0	RF4, RF3, RF2, RF1	All Off
1	1	1	0	0	0	0	1	RF4, RF3, RF2	RF1
1	1	0	1	0	0	1	0	RF4, RF3, RF1	RF2
1	1	0	0	0	0	1	1	RF4, RF3	RF2, RF1
1	0	1	1	0	1	0	0	RF4, RF2, RF1	RF3
1	0	1	0	0	1	0	1	RF4, RF2	RF3, RF1
1	0	0	1	0	1	1	0	RF4, RF1	RF3, RF2
1	0	0	0	0	1	1	1	RF4	RF3, RF2, RF1
0	1	1	1	1	0	0	0	RF3, RF2, RF1	RF4
0	1	1	0	1	0	0	1	RF3, RF2	RF4, RF1
0	1	0	1	1	0	1	0	RF3, RF1	RF4, RF2
0	1	0	0	1	0	1	1	RF3	RF4, RF2, RF1
0	0	1	1	1	1	0	0	RF2, RF1	RF4, RF3
0	0	1	0	1	1	0	1	RF2	RF4, RF3, RF1
0	0	0	1	1	1	1	0	RF1	RF4, RF3, RF2

Register Table

Register 0x0000 – ANT_CTRL0

Bit(s)	Field Name	Description		Reset	B/G	Trig	R/W
7:4	SP4T_SHUNT[3:0]	Shunt Switches - ON		0x0	No	0 - 10	R/W
		0x0: ALL OFF	0x8: RF4				
		0x1: RF1	0x9: RF4, RF1				
		0x2: RF2	0xA: RF4, RF2				
		0x3: RF2, RF1	0xB: RF4, RF2, RF1				
		0x4: RF3	0xC: RF4, RF3				
		0x5: RF3, RF1	0xD: RF4, RF3, RF1				
		0x6: RF3, RF2	0xE: RF4, RF3, RF2				
		0x7: RF3, RF2, RF1	0xF: All On				
3:0	SP4T_SERIES[3:0]	Series Switches - ON		0x0	No	0 - 10	R/W
		0x0: ALL OFF	0x8: RF4				
		0x1: RF1	0x9: RF4, RF1				
		0x2: RF2	0xA: RF4, RF2				
		0x3: RF2, RF1	0xB: RF4, RF2, RF1				
		0x4: RF3	0xC: RF4, RF3				
		0x5: RF3, RF1	0xD: RF4, RF3, RF1				
		0x6: RF3, RF2	0xE: RF4, RF3, RF2				
		0x7: RF3, RF2, RF1	0xF: All On				
		Note: Reg_00 and Reg_01 bits are OR'd together *If Reg_00 is used, do not write to Reg_01, and vice versa*					

Register 0x0001 – ANT_CTRL1

Bit(s)	Field Name	Description		Reset	B/G	Trig	R/W
7:4	SP4T_SHUNT[3:0]	Shunt Switches - ON		0x0	No	0 - 10	R/W
		0x0: ALL OFF	0x8: RF4				
		0x1: RF1	0x9: RF4, RF1				
		0x2: RF2	0xA: RF4, RF2				
		0x3: RF2, RF1	0xB: RF4, RF2, RF1				
		0x4: RF3	0xC: RF4, RF3				
		0x5: RF3, RF1	0xD: RF4, RF3, RF1				
		0x6: RF3, RF2	0xE: RF4, RF3, RF2				
		0x7: RF3, RF2, RF1	0xF: All On				
3:0	SP4T_SERIES[3:0]	Series Switches - ON		0x0	No	0 - 10	R/W
		0x0: ALL OFF	0x8: RF4				
		0x1: RF1	0x9: RF4, RF1				
		0x2: RF2	0xA: RF4, RF2				
		0x3: RF2, RF1	0xB: RF4, RF2, RF1				
		0x4: RF3	0xC: RF4, RF3				
		0x5: RF3, RF1	0xD: RF4, RF3, RF1				
		0x6: RF3, RF2	0xE: RF4, RF3, RF2				
		0x7: RF3, RF2, RF1	0xF: All On				
		Note: Reg_00 and Reg_01 bits are OR'd together *If Reg_00 is used, do not write to Reg_01, and vice versa*					

Register 0x001A – RFFE_STATUS

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	No	No	W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x001B – GSID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x001C – PM_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	PWR_MODE[1]	0: Normal Operation 1: Low Power - Antenna in isolation	1	B/G	No	R/W
6	PWR_MODE[0]	0: ACTIVE 1: STARTUP - Reset all registers to default settings *Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.*	0	B/G	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register.* *If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0b000	No	No	R/W
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.*	0b000	B/G	No	W

Register 0x001D – PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[7:0]	Lower eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x47	No	No	R

Register 0x001E – MANUFACTURER_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	MFG_ID[7:0]	Lower eight bits of MIPI Manufacturer ID *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0xC6	No	No	R

Register 0x001F – MAN_USID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	MFG_ID[11:8]	Upper four bits of MIPI Manufacturer ID *Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.*	0x3	No	No	R
3:0	USID[3:0]	Programmable Unique Slave ID The default value at reset is selected by tying pin SID. SID / USID: VIO 0x6; GND 0x7; float 0x4 *Note: USID is only writeable using a special programming sequence. See MIPI 6.6.2 for details.*	0x7	No	No	R/W

Register 0x0020 – EXT_PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[15:8]	Upper eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x00	No	No	R

Register 0x0021 – REVISION_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	MAJOR_REV[1:0]	Major Revisions - all layer	0b00	No	No	R
5:4	MINOR_REV[1:0]	Minor Revisions - metal only	0b00	No	No	R
3:0	MISC_REV[3:0]	Misc Revisions - mask variants	0b0001	No	No	R
		Note: The REVISION_ID register contains this product's revision number which is set by Qorvo according to manufacture date. The value may change throughout the product life cycle.				

Register 0x0022 – GSID0-1

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x0023 – UDR_RST

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	B/G	No	W
6:0	RESERVED		0x00	No	No	R

Register 0x0024 – ERR_SUM

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	SPARE	Reserved for future use	0	No	No	R/W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

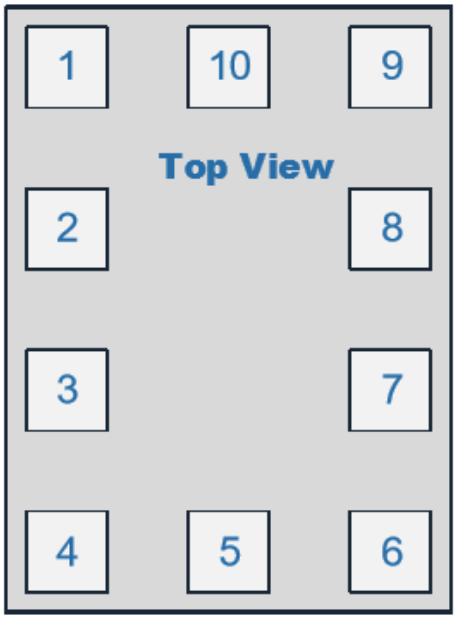
Register 0x002D – EXT_TRIG_MASK

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TriggerMask[10:3]	Setting bit TriggerMask[N] disables Trigger[N] If using an Extended Write to update both TriggerMask and Trigger, than TriggerMask[N] updates before Trigger[N] is processed *Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register.* *If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*	0xFF	No	No	R/W

Register 0x002E – EXT_TRIG

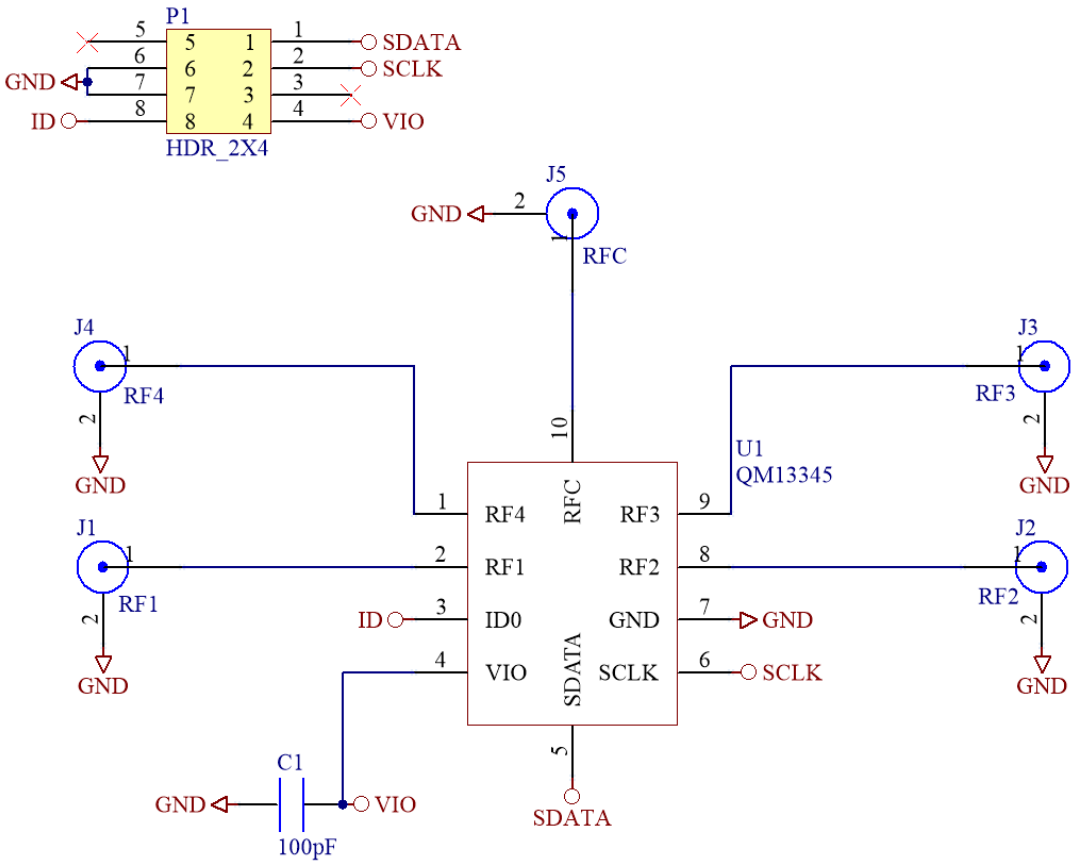
Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	Trigger[10:3]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[10 - 3] will always read as 0.*	0x00	B/G	No	W

Pin Configuration



Pin Number	Label	Description
1	RF4	RF Port 4
2	RF1	RF Port 1
3	ID	USID Pin
4	VIO	VIO Supply
5	SDATA	RFFE SDATA Line
6	SCLK	RFFE SCLK Line
7	GND	Ground
8	RF2	RF Port 2
9	RF3	RF Port 3
10	RFC	RF Common Port

Evaluation Board Schematic and BOM



Part Number	Part	Part Description
U1	QM13345	QM13345, SP4T Switch
J1, J2, J3, J4, J5	SMA connector	Edge mount 0.068” SMA connector
C1	100pF capacitor	(0201) 100pF de-coupling capacitor

DNP components not listed in BOM or shown in schematic

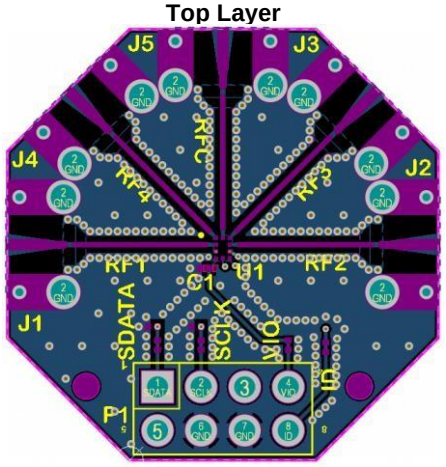
Application Guidelines

Decoupling Capacitors = Decoupling capacitor on VIO may be used for noise reduction. The value of the de-coupling capacitor should be selected based on the application.

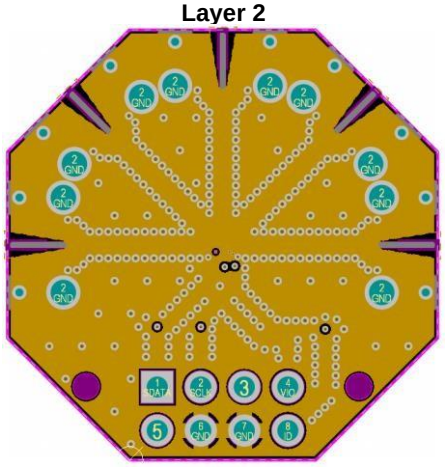
DC Blocking Capacitors = DC blocking capacitor is not required on an RF port if no DC voltage exists on that port

Evaluation Board Layout

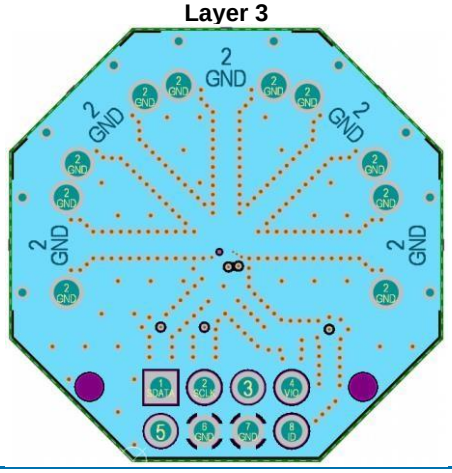
Top Layer



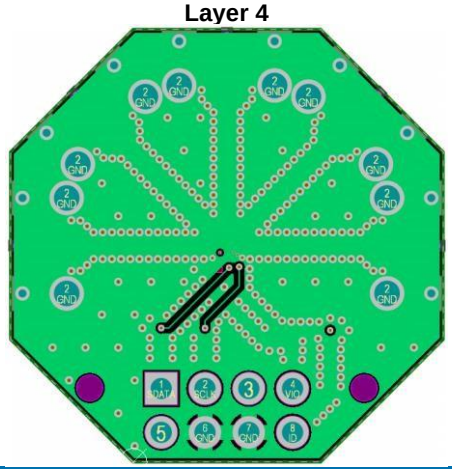
Layer 2



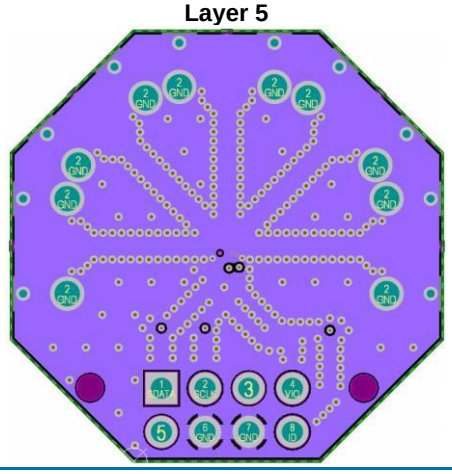
Layer 3



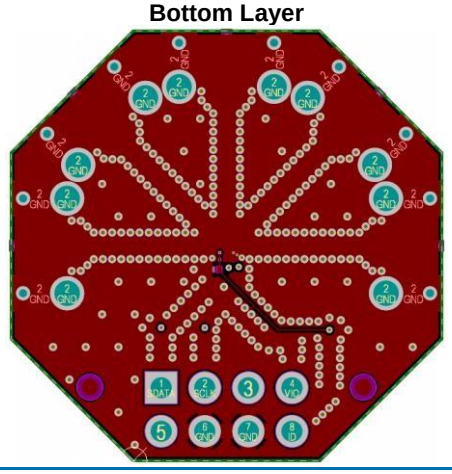
Layer 4



Layer 5

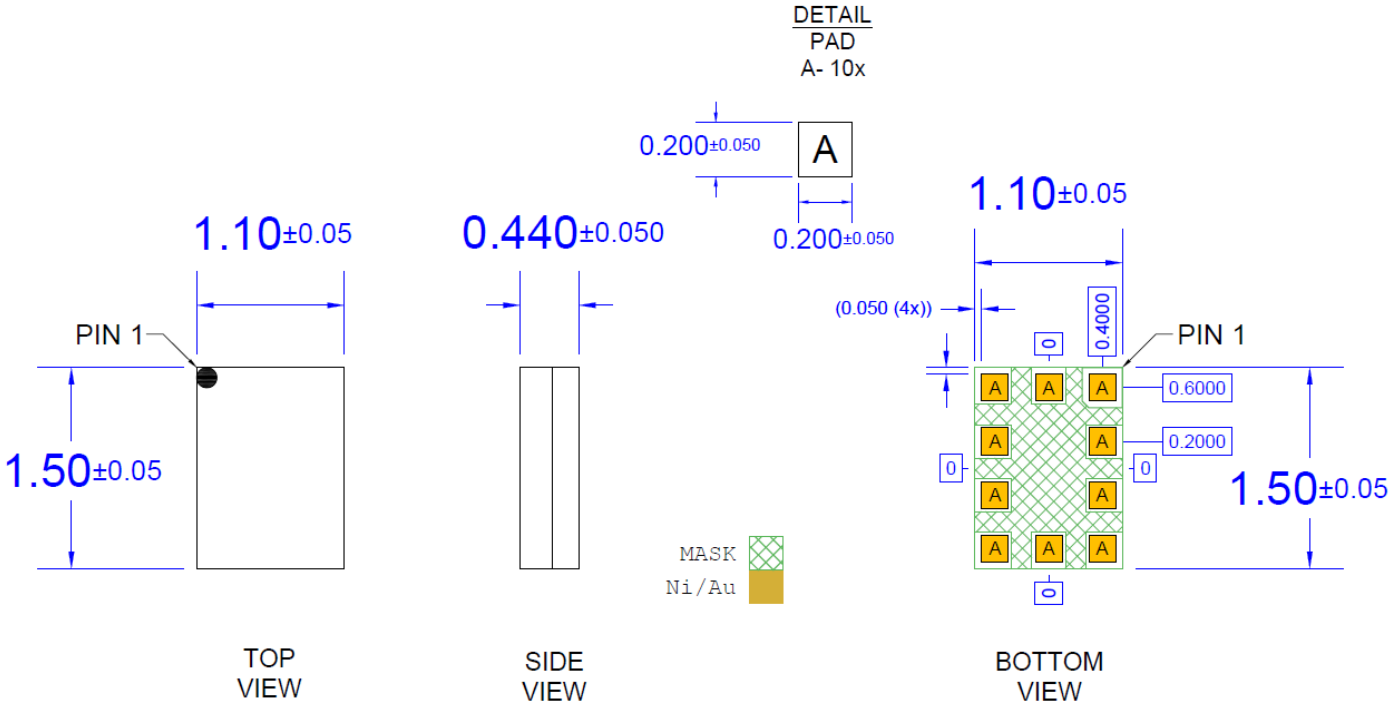


Bottom Layer

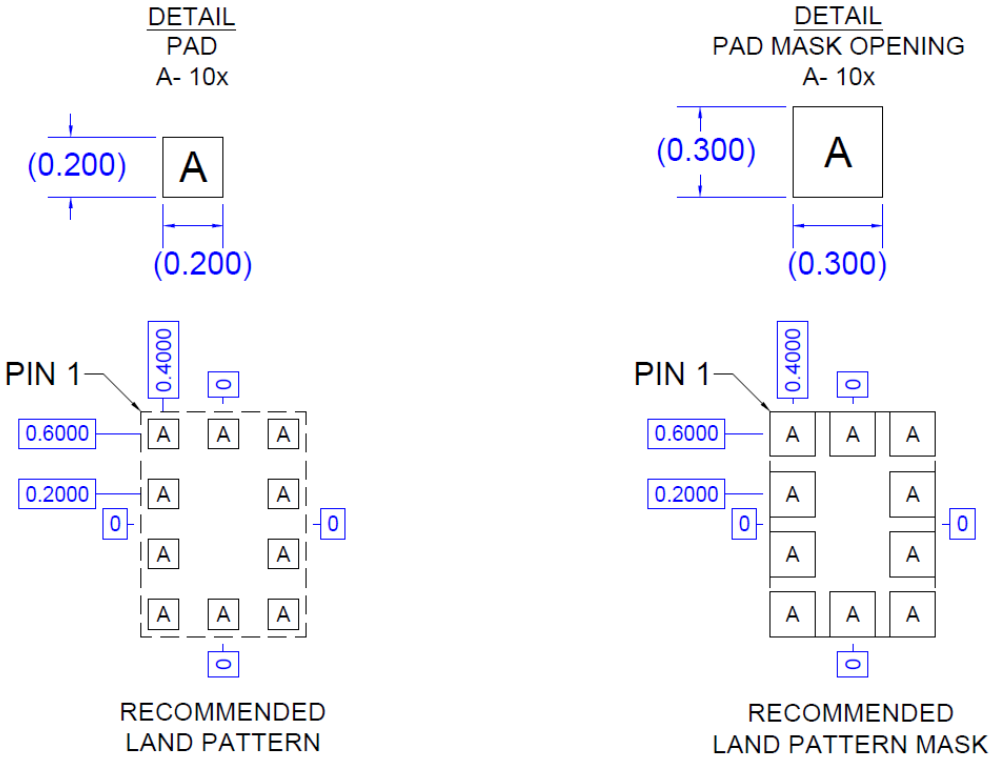


PCB Design Requirement

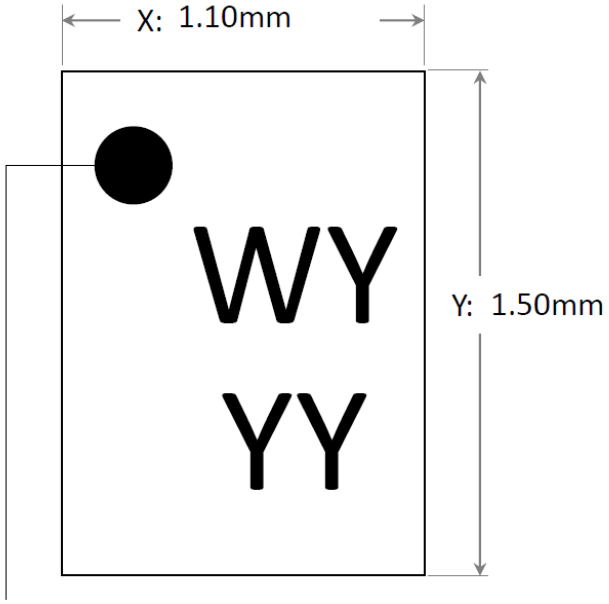
Package Outline Drawing (dimension in mm)



PCB Metal Land Pattern



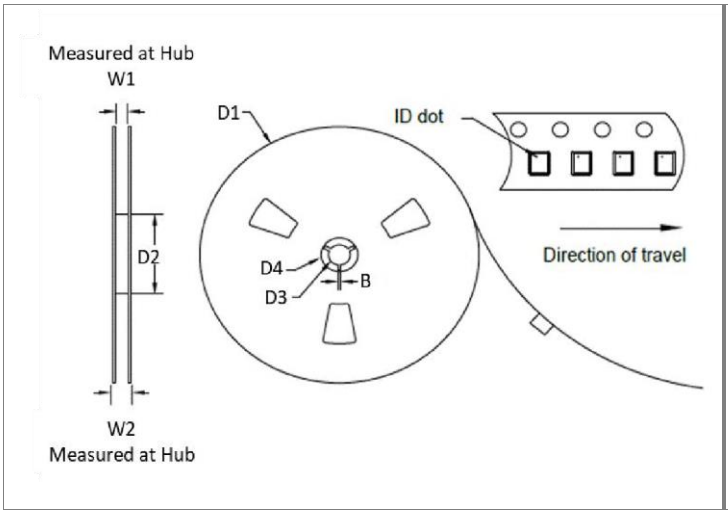
Marking Diagram

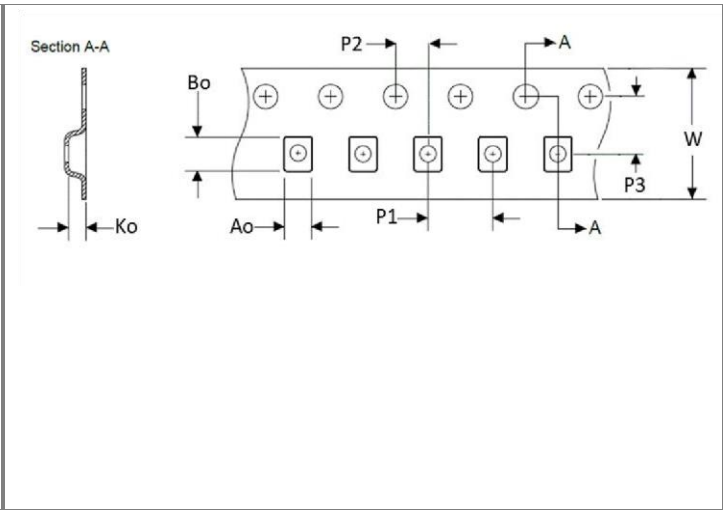


Pin 1 Indicator
Trace Code to be assigned by SubCon

YYY is the Trace Code. "W" is the Product Code.

Tape and Reel





Feature	Measure	Symbol	Size (mm)	Feature	Measure	Symbol	Size (mm)
Flange	Diameter	D1	330.0	Cavity	Length	Ao	1.3
	Thickness	W2	14.2		Width	Bo	1.7
	Space Between Flange	W1	8.8		Depth	Ko	0.6
Hub	Outer Diameter	D2	102.0		Pitch	P1	4.0
	Arbor Hole Diameter	D3	13.0	Centerline Distance	Cavity to Perforation (Length)	P2	2.0
	Key Slit Width	B	2.0		Cavity to Perforation (Width)	P3	3.5
	Key Slit Diameter	D4	20.2	Carrier Tape	Width	W	8.0

Handling Precautions

PARAMETER	VALUE	STANDARD
ESD – Human Body Model (HBM)	Class 2	ESDA/JEDEC JS-001
ESD – Charged Device Model (CMD)	Class C3	ESDA/JEDEC JS-002
Moisture Sensitivity Level (MSL)	MSL 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C max. reflow temperature) and tin/lead (245 °C max. reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

Revision History

REVISION	RELEASE DATE	DESCRIPTION
H	12/10/2020	Initial Production Release
I	9/1/2021	Update Performance, Timing Diagrams, ESD, MSL

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:
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Email: customer.support@qorvo.com

Important Notice

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