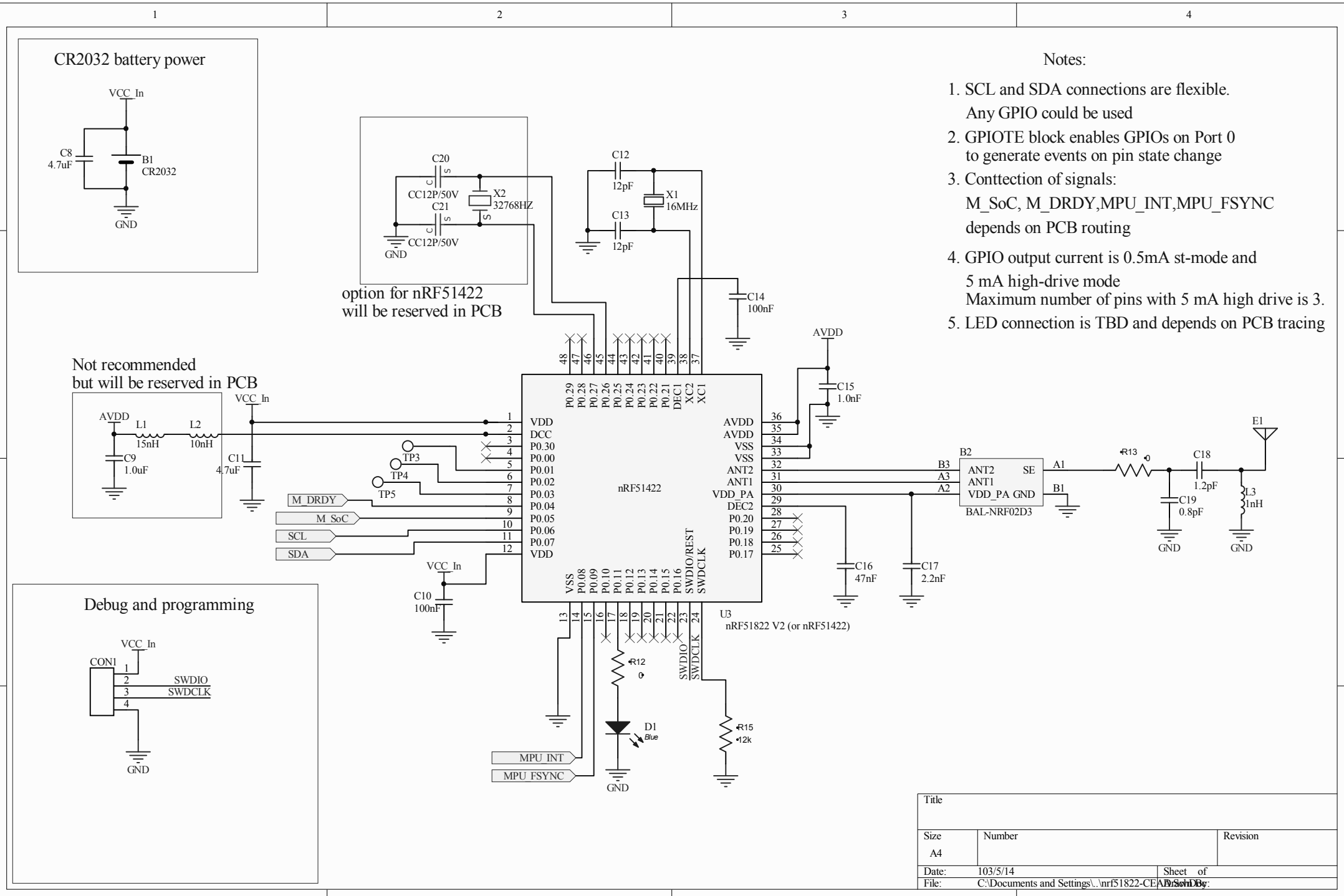
CR2032 battery power
VCC_In
C8
4.7uF
B1
CR2032
GND
C20
CC12P/50V
C21
CC12P/50V
X2
32768HZ
GND
option for nRF51422
will be reserved in PCB
C12
12pF
C13
12pF
X1
16MHz
C14
100nF
AVDD
C15
1.0nF
Not recommended
but will be reserved in PCB
AVDD
L1
15nH
L2
10nH
C9
1.0uF
VCC_In
C11
4.7uF
TP3
TP4
TP5
M_DRDY
M_SoC
SCL
SDA
VCC_In
C10
100nF
nRF51422
VDD
DCC
P0.30
P0.00
P0.01
P0.02
P0.03
P0.04
P0.05
P0.06
P0.07
VDD
AVDD
AVDD
VSS
VSS
ANT2
ANT1
VDD_PA
DEC2
P0.20
P0.19
P0.18
P0.17
VSS
P0.08
P0.09
P0.10
P0.11
P0.12
P0.13
P0.14
P0.15
P0.16
SWDIO/REST
SWDCLK
U3
nRF51822 V2 (or nRF51422)
B2
ANT2
ANT1
VDD_PA
SE
GND
BAL-NRF02D3
B3
A3
A2
A1
B1
R13
0
C18
1.2pF
C19
0.8pF
L3
1nH
E1
GND
GND
C16
47nF
C17
2.2nF
R12
0
D1
Blue
GND
R15
12k
MPU_INT
MPU_FSYNC
SWDIO
SWDCLK
Debug and programming
VCC_In
CON1
SWDIO
SWDCLK
GND
Notes:
1. SCL and SDA connections are flexible.
Any GPIO could be used
2. GPIOTE block enables GPIOs on Port 0
to generate events on pin state change
3. Conttection of signals:
M_SoC, M_DRDY,MPU_INT,MPU_FSYNC
depends on PCB routing
4. GPIO output current is 0.5mA st-mode and
5 mA high-drive mode
Maximum number of pins with 5 mA high drive is 3.
5. LED connection is TBD and depends on PCB tracing
Title
Size
A4
Number
Revision
Date: 103/5/14
Sheet of
File: C:\Documents and Settings\..\nrf51822-CEA.SchDoc
Drawn By: