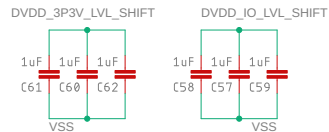
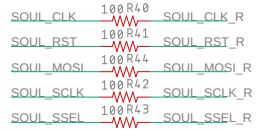
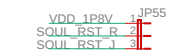
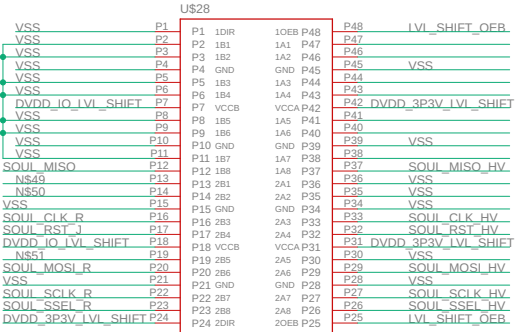
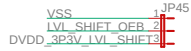
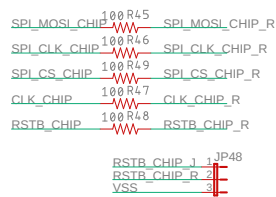
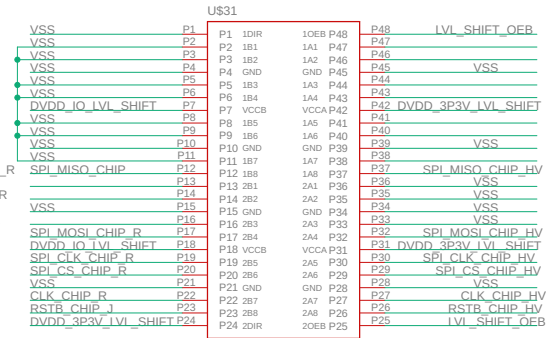
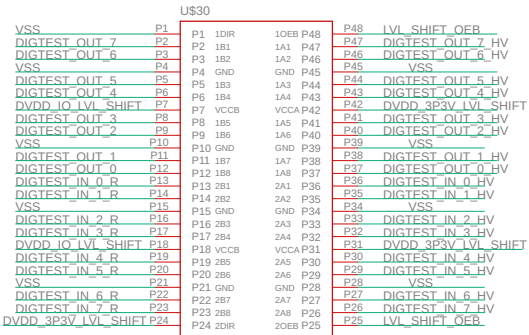
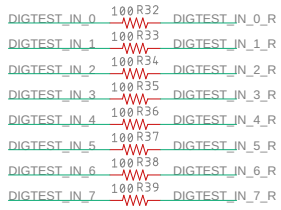


Jumpers so that Adel can easily measure current going into his DVDD_SOUL pin in any way he wants

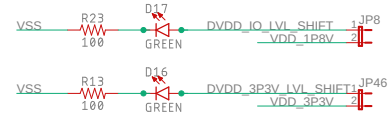
These Vcm caps may be left unpopulated or their values may change depending on our Vcm needs

Ear EEG IC

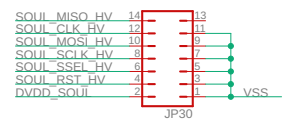


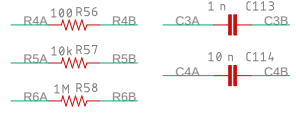
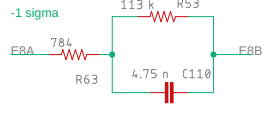
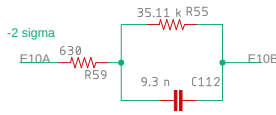
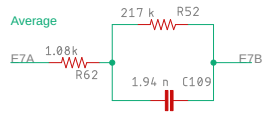
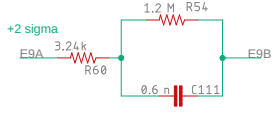
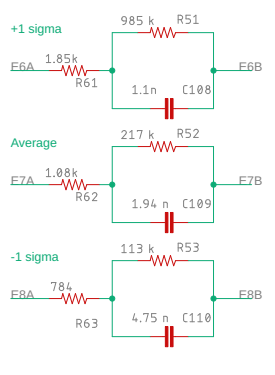
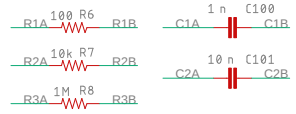
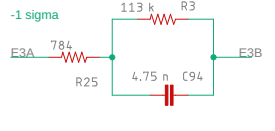
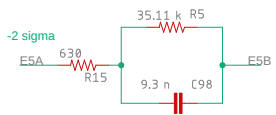
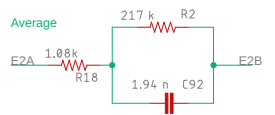
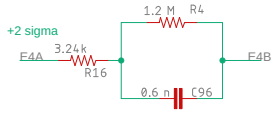
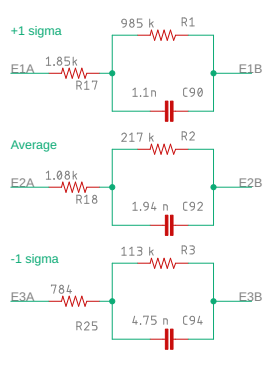
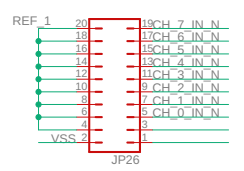
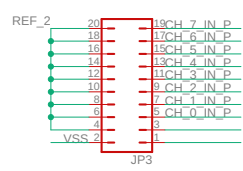
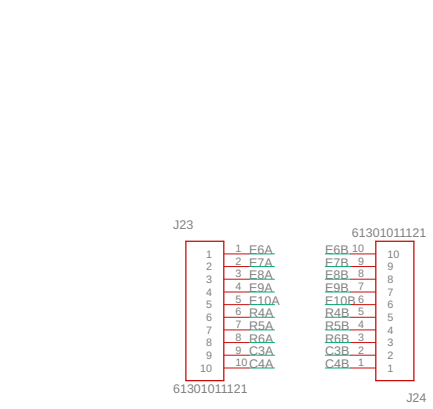
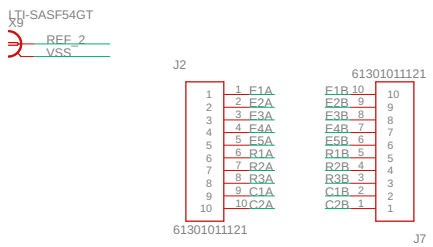
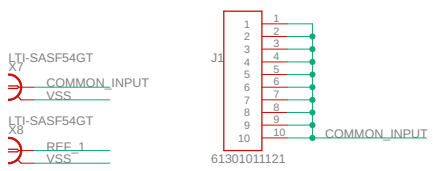
All these chips will be right next to each other so we will try to share a single set of decap.

We can add more if people want.



Level Shifters





Input headers with electrode models

Pin out some FPGA pins just in case

FPGA GPIO pins for switches and LEDs

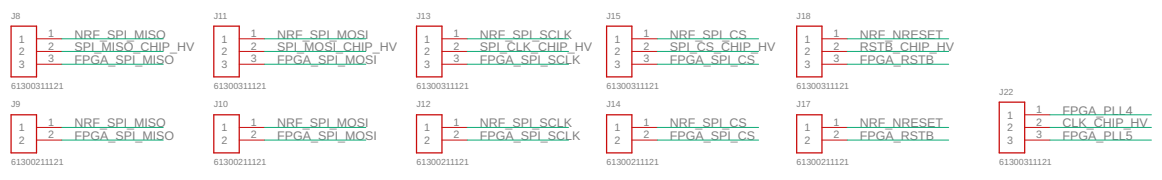
J4			
VSS	01	02	VDD_EPGA
	03	04	VDD_EPGA
	05	06	VDD_EPGA
	07	08	
FPGA_PLL4	09	10	
VSS	11	12	
	13	14	VSS
	15	16	
	17	18	
	19	20	
	21	22	
	23	24	
	25	26	
	27	28	
	29	30	
	31	32	
	33	34	
	35	36	VSS
	37	38	
	39	40	
SOUL_MISO_HV	41	42	FPGA_SPI_CS
SOUL_CLK_HV	43	44	FPGA_SPI_SCLK
SOUL_MOSI_HV	45	46	FPGA_SPI_MISO
SOUL_SCLK_HV	47	48	FPGA_SPI_MOSI
SOUL_SS1_HV	49	50	
SOUL_RST_HV	51	52	
	53	54	
	55	56	VSS
	57	58	61300811121
	59	60	8
	61	62	K21 7
	63	64	K22 6
E21	65	66	G20 5
F22	67	68	G22 4
D21	69	70	E20 3
	71	72	E22 2
	73	74	C22 1
	75	76	
	77	78	VSS
	79	80	VSS

BTE-040-01-F-D-A
JP2

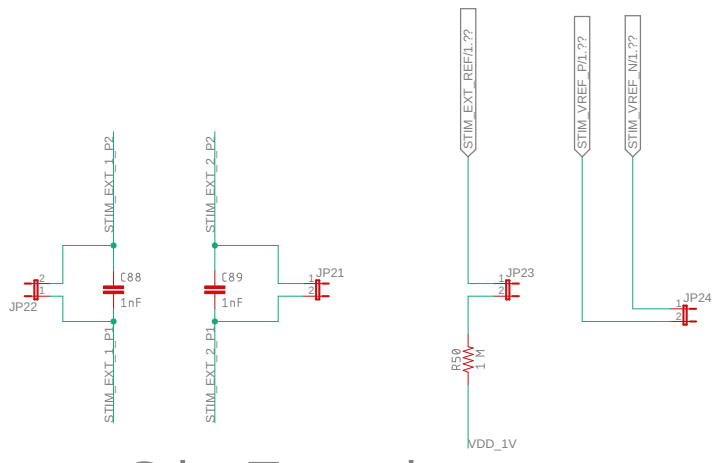
J5			
	01	02	VSS
	03	04	
	05	06	
	07	08	FPGA_PLL5
	09	10	
	11	12	
	13	14	VSS
DIGTEST_IN_7_EPGA	15	16	
DIGTEST_IN_6_EPGA	17	18	
DIGTEST_IN_5_EPGA	19	20	
DIGTEST_IN_4_EPGA	21	22	
DIGTEST_IN_3_EPGA	23	24	
DIGTEST_IN_2_EPGA	25	26	
DIGTEST_IN_1_EPGA	27	28	
DIGTEST_IN_0_EPGA	29	30	
	31	32	
	33	34	
VSS	35	36	
	37	38	
	39	40	
	41	42	
	43	44	
	45	46	
SYNC	47	48	
EPGA_RSTB	49	50	
	51	52	
	53	54	
VSS	55	56	
DIGTEST_OUT_0_EPGA	57	58	
	59	60	
	61	62	
DIGTEST_OUT_1_EPGA	63	64	
DIGTEST_OUT_2_EPGA	65	66	
DIGTEST_OUT_3_EPGA	67	68	
DIGTEST_OUT_4_EPGA	69	70	A14
DIGTEST_OUT_5_EPGA	71	72	B16
DIGTEST_OUT_6_EPGA	73	74	A16
DIGTEST_OUT_7_EPGA	75	76	B18
	77	78	VSS
	79	80	VSS

BTE-040-01-F-D-A
JP3

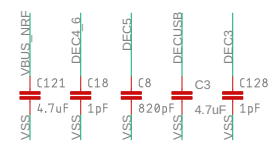
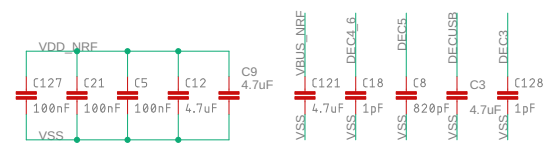
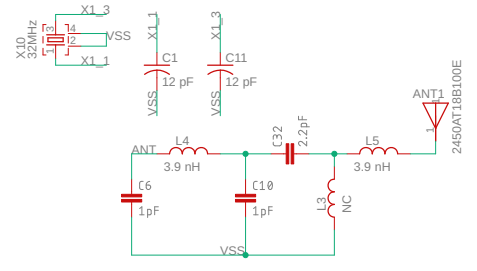
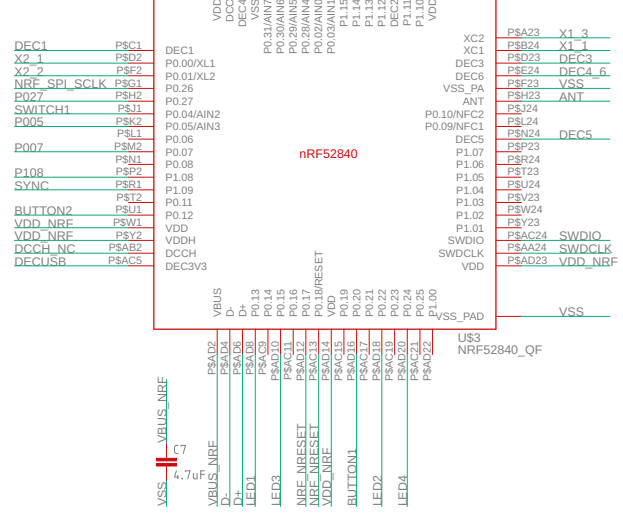
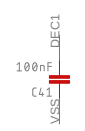
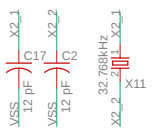
FPGA headers



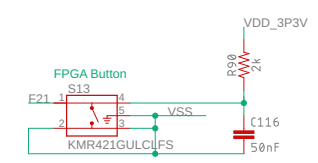
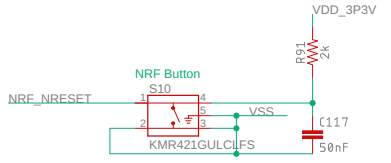
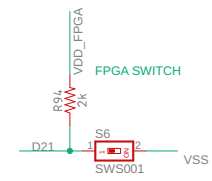
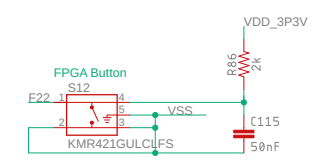
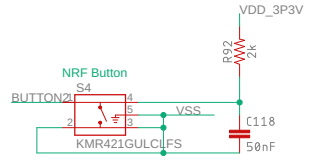
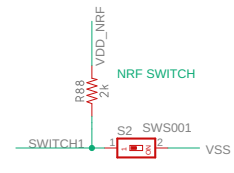
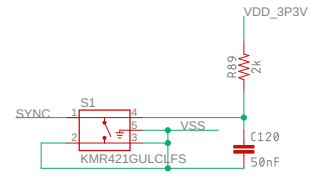
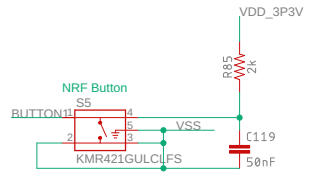
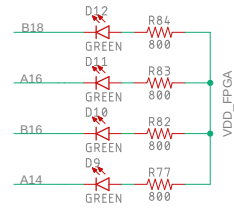
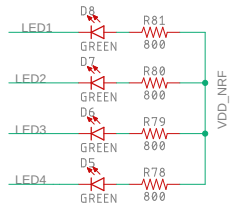
Digtest & various jumpers



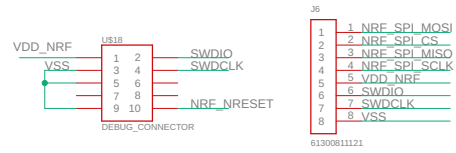
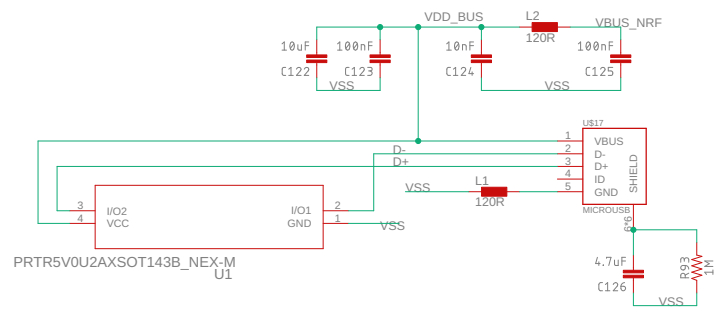
Stim Testpoints



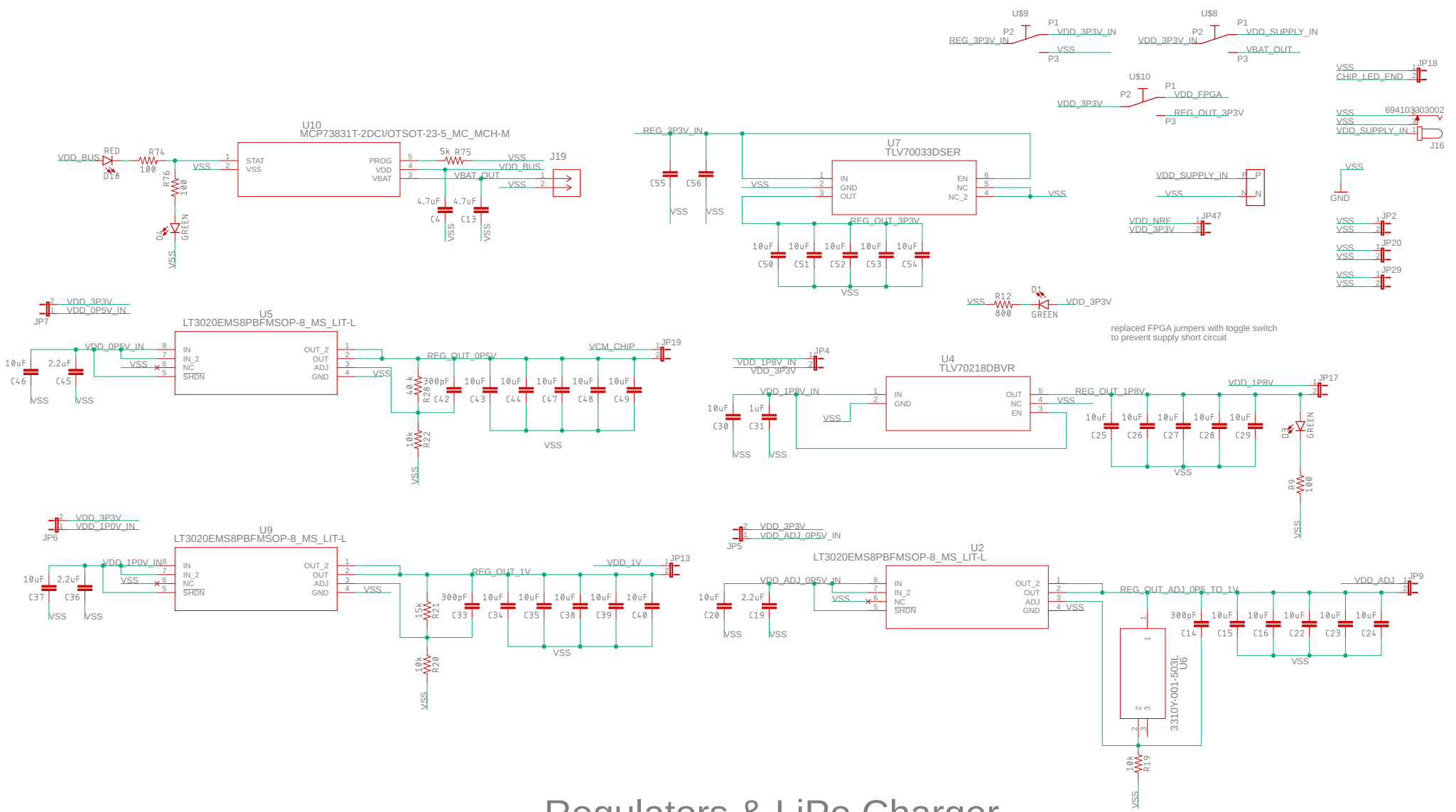
Nordic IC



GPIO LEDS & Switches



Headers for NRF USB, Programming, & SPI



Regulators & LiPo Charger