MAX30003WING

High Level Design

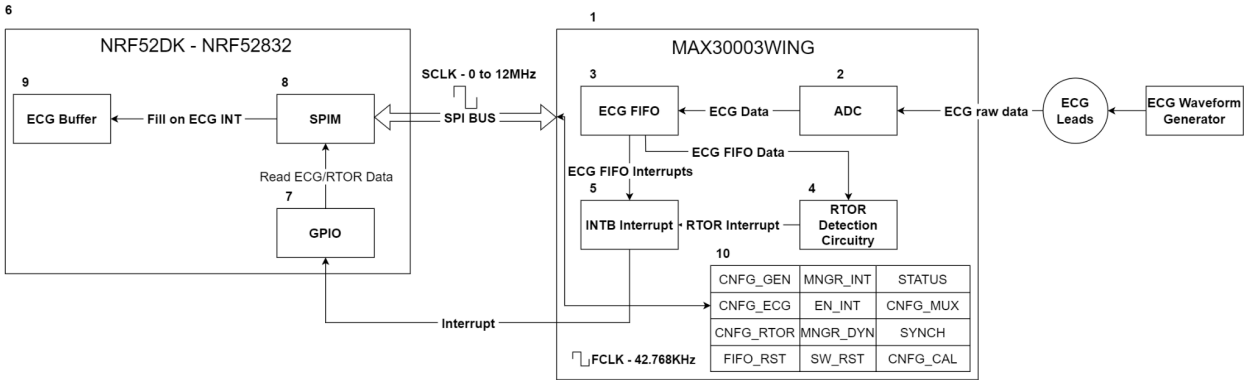

Fig A

1 - MAX30003WING

A. MAX30003WING uses an internal clock (FCLK - 32.768KHz) that is configurable using SPI to synchronize the internal operation of the MAX30003 Chip.

B. It has a FIFO buffer to fill the ECG data, ADC to measure the input signal, R to R detection circuit, Leads off Detection, sequencing circuits to control the ECG FIFO head and tail Pointers.

2 - ADC

A. The ADC samples the input signal at various rates such as 512, 128, 127 et cetera based on the configured registers and stores the samples in the FIFO buffer asynchronously. It also can be configured to generate an interrupt on the INTB pin whenever an R Peak occurs.

3 - ECG FIFO Buffer

A. Once the set number of samples(in the EFIT field of EN_INT register) is filled, it is configured to generate an interrupt in the INTB pin of the board.

B. Once the ECG Sample is read, the buffer head pointer is automatically incremented on the 30th clock pulse of that read operation. Tail pointer is automatically incremented and wrapped back to 0.

C. Size of the buffer = 32 * 24 bits where each 24 bits = 18 bit ECG Value + 3 bit ETAG + 3 bit PTAG

4 - R-TO-R Detection

A. R-To-R circuit determines R peaks. It can be configured to trigger INTB interrupt whenever it detects R peaks. R-to-R register deals with configuration related to R peaks

5 - Active Low INTB Interrupt Pin

A. INTB Interrupt is the interrupt pin of MAX30003 which throws any type of system interrupts that includes but is not limited to FIFO related interrupts(E_INT), R-to-R interrupt, Leads-off/on interrupt.

6 - Nordic NRF52DK-NRF52832

A. Host MCU dev board to run application code that communicates with MAX30003WING

7 - GPIO Pin to detect INTB Interrupt

A. After an interrupt, the STATUS register is read to see the type of interrupt that triggered INTB pin

B. If the interrupt is EN_INT(ECG FIFO threshold samples full), ECG Samples are read back until the last sample (indicated by ETAG as part of the read ECG FIFO DATA)
C. If it is an R-to-R interrupt, R-to-R register is read and Heart rate is calculated
D. Leads-off and Leads-on detection with varying current sources can be enabled. If enabled, it can be configured to generate an INTB interrupt using the EN_INT register

8 - SPIM Interface

A. SPIM library in Nordic is used to interact with the MAX30003WING board using MISO, MOSI, SCLK, SSEL pins. SSEL pin is active low.

9 - ECG Buffer

A. ECG buffer used to store MAX30003WING's n * 24 bit ECG FIFO data where n is equal to EFIT configured previously in the EN_INT register.

10 - MAX30003 Registers

A. MAX30003's internal operation can be controlled by a set of registers like CNF_GEN, MNGR_DYN, STATUS et cetera. For preferred configuration, refer to Fig F.Register Configuration

Pins Needed

- MAXIM30003: SPI (miso, mosi, vcc, gnd, ssel, sclk), Interrupt B(INTB)
- Nordic NRF52 DK: SPI(miso, mosi, vcc, gnd, ssel, sclk), GPIO pin for INTB
- ECG leads: Left/tip - ECGP -> Wave generator +ve, Right/ring - ECGN-> Wave generator -Ve, Ground/sleeve - VCM -> Ground
  Body bias(optionally connected to body ground)

Parameters & Constraints

- MAXIM30003 SPI CLK range - 0 to 12 MHz
- SSEL - Active Low
- INTB - Active Low
- Maxim Internal Clock - 32.768KHz(configurable in register)
- MAXIM FIFO Size - 32 words each of 24 bits
- Input ECG Freq - 1Hz
- Tested ECG Signal Amplitude range 1mVpp - 100mvpp

Fig B

Input Waveform

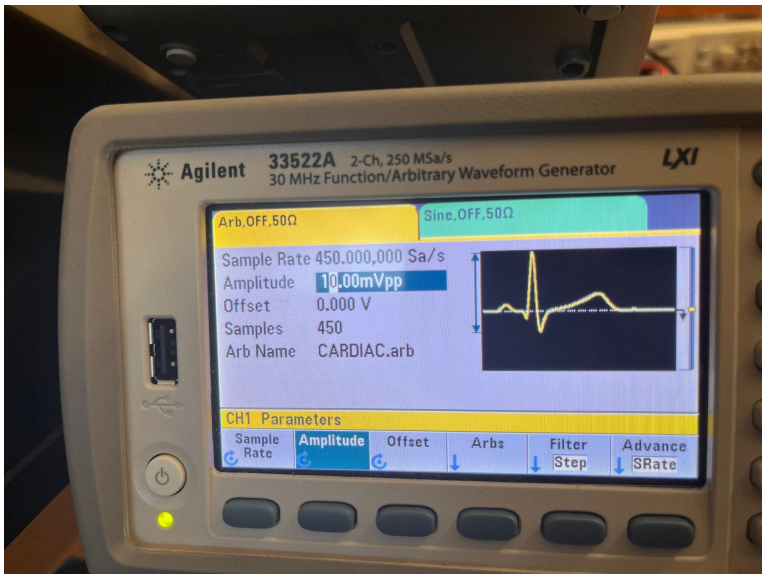

Fig C

Setup

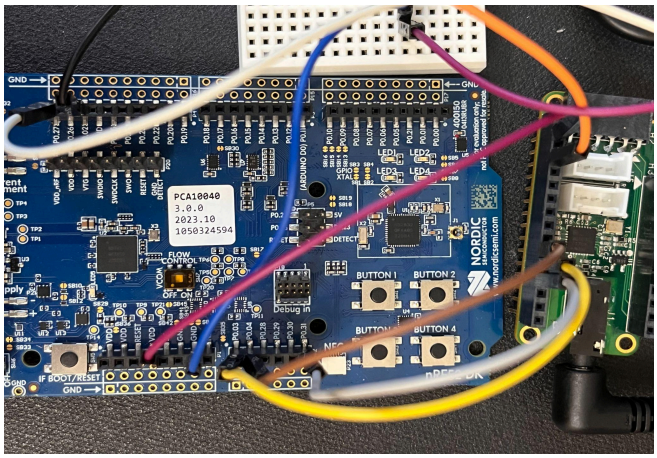

Fig D

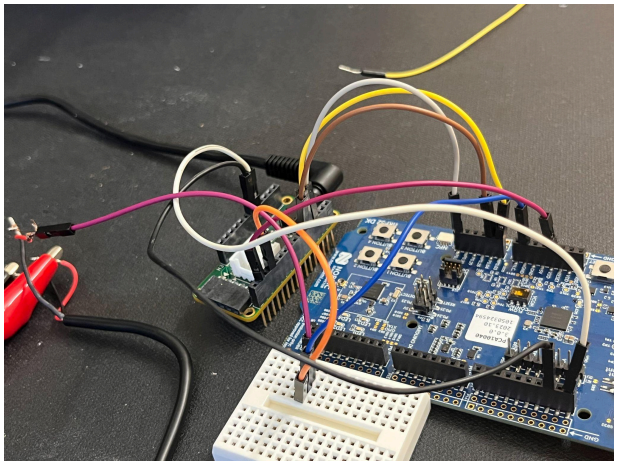

Fig E

Software

1. Initialize the SPI interface in Nordic with SPI pins and allowed frequency for SCLK(4MHz by default)
2. Initialize a GPIO Pin(p0.027) to connect to INTB pin on the MAX30003WING and add a callback to toggle the intB flag whenever there is an interrupt from the INTB pin
3. SW_RST register is written with a value of 0 to reset the board to initial conditions.
4. Configure the following Maxim30003 registers like CNFG_GEN, CNFG_ECG, CNFG_RTOR, MNG_INT, EN_INT, MNG_DYN_r, CNFG_MUX, CAL_CONFG

Fig F

Register	Component	Value
CNFG_GEN	Enable ecg channel	1
	Resistive bias on -ve input	1
	Resistive bias on +ve input	1
	Resistive bias	1
	DC leads off current source Magnitude	10A
	DCLeads off Detection Enable	1
CNFG_ECG	DLP(Low Pass cut off)	40Hz
	DHP(High Pass cut off)	0.5Hz
	gain	160V/V
	rate	512/128
CNFG_RTOR	Window	96ms
	r_to_r enable	1
	Auto scale gain	15(Auto - default)
	Peak Averaging Factor	0b11 - (16)
	Peak threshold scaling factor	0b11 - default
	Enable r_to_r	1
MNG_INT	EFIT - ECG FIFO Interrupt Threshold	16 - 16 samples
	Clear RR INT	1 (Clear RR_INT on status register read back)
EN_INT(governs INTB)	Enable EINT	1(throws interrupt when EFIT samples are full)
	Enable RRINT	1(throws interrupt when R event occur)
	INTB_TYPE	3 (INTB pin is configured with 125k pull up resistor)
MNG_DYN	Fast Recovery Mode	Disabled

CNFG_MUX	openn(connect ECGN to AFE channel)	0 - connect/1-isolate
	openp(connect ECGP to AFE channel)	0 - connect/1-isolate

5. Set SYNCH register to 0. SYNCH (Synchronize) is a write-only register/command that begins new ECG operations and recording, beginning on the internal MSTR clock edge following the end of the SPI SYNCH transaction (i.e. the 32nd SCLK rising edge).
6. INTB interrupt is triggered whenever the FIFO is filled with EFIT number of samples or R peak is detected.
7. On INTB Interrupt, read STATUS register to check the type of interrupt
8. For RTOR interrupt, extract RTOR and calculate BPM as shown in control flow
9. For FIFO interrupt, read 24 bit FIFO data until ETAG represents EOF.
   9.1 24 bits FIFO Data = 18 bits ECG Data + 3 bits ETAG + 3 bits PTAG with PTAG starting at LSB(0)
   9.2 Extract ECG data using a) fifo_data << 8 or b) fifo_data << 6
   9.3 Implicitly, 16 samples should be read as EFIT is 16
   9.4 If FIFO overflow occurs, FIFO_RST register is written with a value of 0. This resets the FIFO memories and resumes the record with the next available ECG data.

Synchronization

Timing characteristics

- MAXIM30003 ECG FIFO Buffer is filled with 512 sa/s. Every Sample is filled in a 1.95ms(1000ms/512) time period.
- Since SCLK is 4MHZ, positive pulse width is 0.125us assuming 50% duty cycle.
- Single ECG FIFO read = 0.125us x 32bits(8 bit address + 24 data bits) = 4us
- 16 ECG sample read = 4 x 16 = 64us
- Time to read single ECG Sample in while loop = 400us
- Time to read 512 Samples in Nordic = 996ms