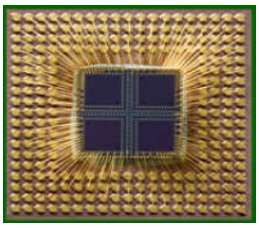
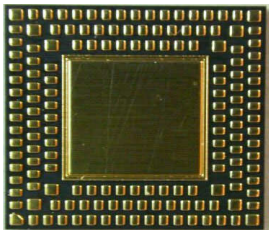
ASE GROUP

AQFN Surface Mount Application Notes





Date:2013.02.26

Prepare By: CPE/SMT team

Contents:

1.0 **Abstract**

Quad Flat No Lead (QFN) is a lead-frame based plastic package, it has several advantages over traditional lead-frame package, that include reduced lead inductance, a near chip scale size offers improving electrical performance and lower weight, it use perimeter I/O pads to ease PCB trace routing, and exposed copper die-pad technology to offer good thermal performance. These features make QFN an ideal choice for many new applications where size, weight, thermal and electrical performance are important.

What is aQFN? it is based on existing etching lead-frame & IC assembly process to develop new technology , and it is also similar but different to QFN process, It's key concept is on Leadless, Pb-free & multi-row package, and due to its stand-off structure, let it get more benefits in surface mount reliability, so it has QFN all advantage and create more features than QFN.

The features of aQFN have:
- Low profile, small footprint and light weight
- Free-form I/O design
- Fine lead pitch 0.4mm
- Excellent thermal performance
- Excellent electrical performance
- Cost effective package
- Extend QFN I/O count up to 300

2.0 Surface Mount Consideration

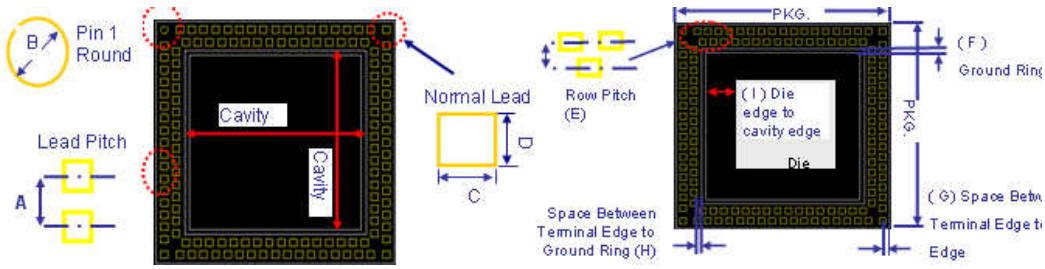
For getting good performance on thermal, electrical, board level when user do surface mount assembly, some factors need to consider, such as PCB design, stencil design, type of solder paste, component placement consideration, reflow profile setting, and assembly process flow. This application notes just provide guideline for user reference, hope this guideline could help user in developing the proper mother board design and surface mount process.

3.0 PCB Design Requirements

3.1 Package Outline **(POD)** Information

ITEM	Symbol	NORMAL
Lead Pitch	A	0.8 / 0.65 / 0.5
Pin 1 Diameter is Round	B	Min= 0.23
Lead Dimension - X	C	Min= 0.23
Lead Dimension - Y	D	Min= 0.23

Terminal Size should >= 0.23mm (Testing limitation)



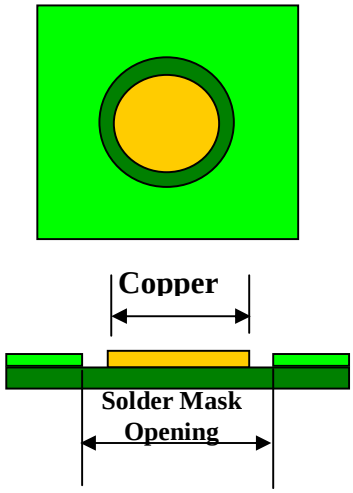
ITEM	Symbol	NORMAL
Row Pitch	E	D + 0.2
Ground Ring	F	0.2
Space between terminal edge to PKG edge	G	0.2
Space between terminal edge to ground ring	H	0.25
Die edge to cavity edge	I	0.3

3.2 Land Pattern Design **(ref. IPC-SM-7351A or -782)**

There are two types of land patterns are chosen for user PCB design, one is Solder Mask Defined (SMD), solder mask openings smaller than metal pads. The other is Non-Solder Mask Defined (NSMD), solder mask openings larger than metal pads. Better control of the copper etching process as compared to the solder masking process makes NSMD preferable. Also, the SMD pad definition can introduce stress concentrations near the solder mask overlap region that can result in solder joints cracking under extreme fatigue conditions. Using NSMD instead improves the reliability of solder joints as solder is allowed to "wrap around" the sides of the metal pads on the board

Base on real SMT assembly test, NSMD and circle shape is recommended to use on SMT assembly, the pad size defined as below showing:

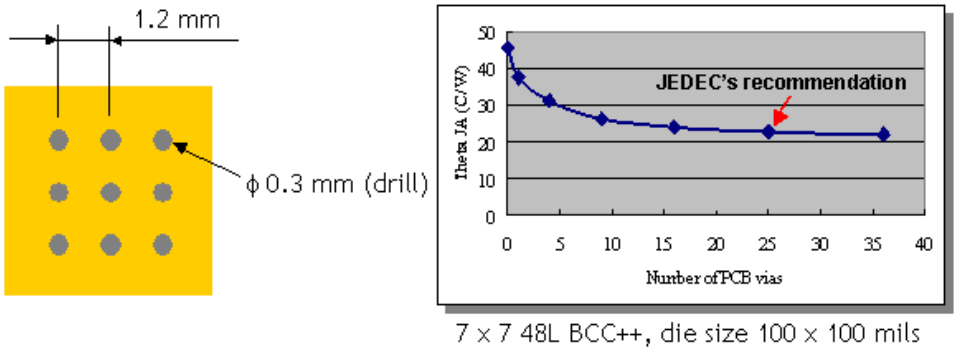
NSMD(Non-Solder Mask Defined)



aQFN Package			PCB Land Pad Design		
Land Pitch	Terminal Size	Land Shape	Land Shape	Copper Pad	Solder Mask
0.65 mm	0.35 mm	Circle	Circle	0.375mm	0.475mm
0.5 mm	0.23 mm	Circle	Circle	0.255mm	0.355mm

3.3 Thermal Via Design **(ref. JEDEC 51-5)**

In order to transfer the heat from top of later on PCB to inner or bottom layer, thermal via design is necessary. Base on JEDEC recommendation, the design with via diameter 0.3mm and pitch 1.2mm is a better design. The numbers of thermal via more than this design just can help a little on the thermal performance, as below showing of simulation data:



7 x 7 48L BCC++, die size 100 x 100 mils

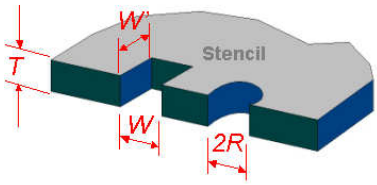
3.4 Thermal Pad and Power Ring Design:

Thermal Pad and Power Ring Design for PCB, ASE suggest 1:1 as package size, to make PCB' thermal pad and power ring dimension as same as aQFN package design.

4.0 Board Mounting Guidelines

4.1 Stencil Design

4.1.1 Basic concept: Aspect Ratio (W/T, 2R/T) > 1.5, Area Ratio (W/4T, R/2T) > 66%



4.1.2 Trapezoidal Aperture: Bottom Opening 25~50 microns larger than the Top, Well design for paste release

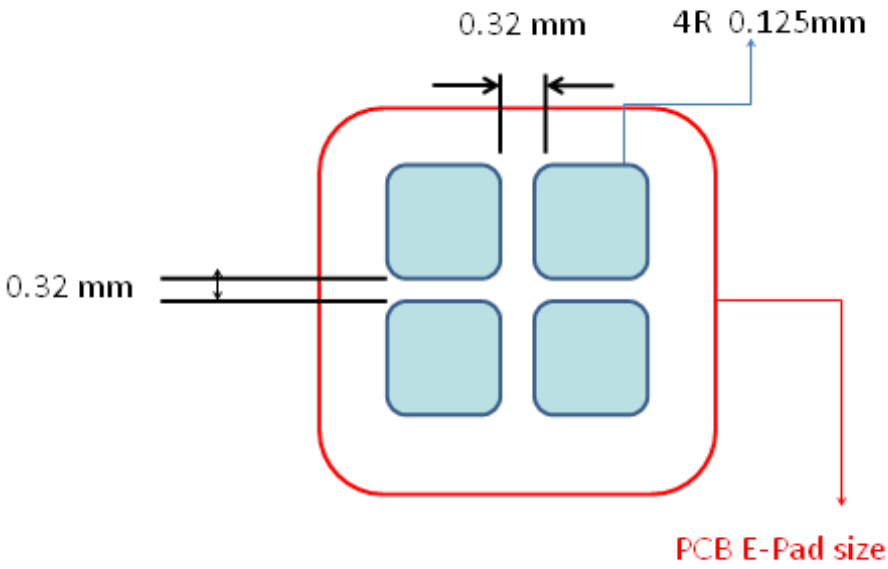
4.1.3 Use laser cutting followed by electro-polishing for stencil fabrication.

4.1.4 The recommended stencil apertures are same with PCB land pattern, Thickness is 0.1mm

4.1.5 Use Type 4 solder paste(25 to 45 micron particle size range) or finer for solder printing, and SAC305 is common used solder paste. Senju M705-S101-S4 is recommended solder paste.

4.1.6 For thermal paddle stencil opening, **using array of 2X2 opening and 20% opening of PCB thermal paddle area is recommend** to avoid void resident inside thermal paddle and can get better solderability

Recommend of stencil opening of thermal paddle



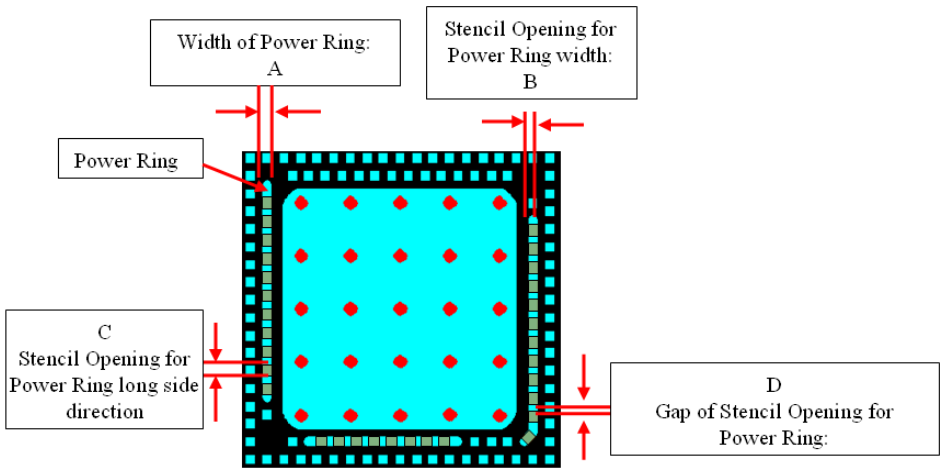
Rule:

1. Total opening area of stencil/ Total area of PCB's thermal pad = 20%

Stencil Recommend Opening

aQFN Package			PCB Land Pad Design			Stencil		
Land Pitch	Terminal Size	Land Shape	Land Shape	Copper Pad	Solder Mask	Thickness	Shap	Opening
0.65 mm	0.35 mm	Circle	Circle	0.375mm	0.475mm	0.12 mm	Circle	0.4 mm
0.5 mm	0.23 mm	Circle	Circle	0.255mm	0.355mm	0.1 mm	Circle	0.27 mm

4.1.7 For power ring, stencil opening describe as below drawing:



Rule:

1. **A = B**
2. **0.3mm < C < 0.6mm**
3. **D > 0.2mm**

4.2 Component Placement

For placing the aQFN, following methods can be used for recognition and positioning

4.2.1 Vision system to locate package outline.

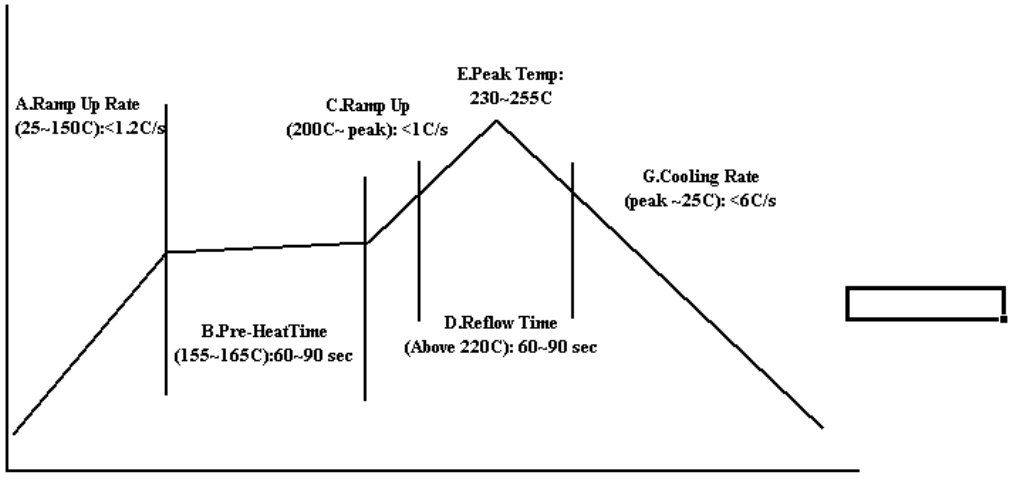
4.2.2 Vision system to locate individual bumps. It is recommended that the side-lighting option on the pick and place machine's vision system be used when attempting to use a individual bump recognition approach to ensure better contrast for bump recognition

4.2.3 It is prefer to use machine with fine pitch placement for better accuracy

4.3 Reflow Proflie

Below reflow-profile is base on using solder paste SAC305

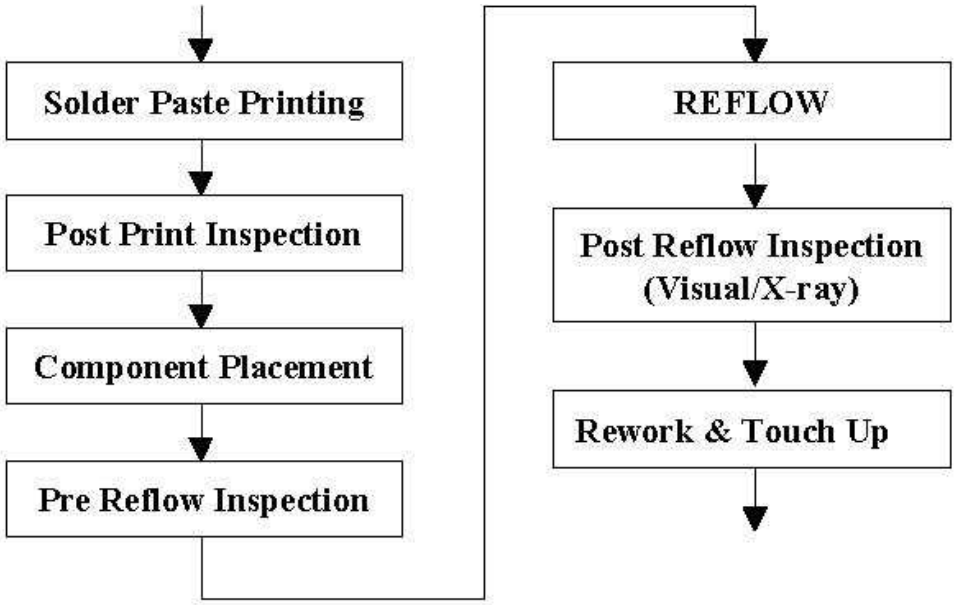
	A.Ramp Up Rate (25~150C)	B.Pre-HeatTime (155~165C)	C.Ramp Up (200C~ peak)	D.Reflow Time (Above 220C)	E.Peak Temp	G.Cooling Rate (peak ~25C)
SPEC.	<1.2C/s	60~90 sec	<1C/s	60~90 sec	230~255C	<6C/s



5.0 Assembly Process Flow

Below Figure shows the typical process flow for mounting surface mount packages to printed circuit boards. The same process can be used for mounting the aQFN without any modifications. It is important to include post print and post reflow inspection, especially during process development. The volume of paste printed should be measured either by 2D or 3D techniques. The paste volume should be around 80 to 90% of stencil aperture volume to indicate good paste release. After reflow, the mounted package should be inspected in transmission x-ray for the presence of voids, solder balling, solder bridge or other defects. Cross-sectioning may also be required to determine solder joint situation.

Typical reflow profiles for No Clean solder paste are shown in 4.3. Since the actual reflow profile depends on the solder paste being used and the board density, ASE does not recommend a specific profile. However, the temperature should not exceed the maximum temperature the package is qualified for according to moisture sensitivity level. The time above liquidus temperature should be around 70 seconds and the ramp rate during preheat should be 1 ^{o}C/second or lower.



6.0 Rework Process (ref. IPC-7711)

For defects underneath the package, the whole package has to be removed. Rework of aQFN packages can be a challenge due to their small size. In most applications, aQFN will be mounted on smaller, thinner, and denser PCBs that introduces further challenges due to handling and heating issues. Since reflow of adjacent parts is not desirable during rework, the proximity of other components may further complicate this process. Because of the product dependent complexities, the following only provides a guideline and a starting point for the development of a successful rework process for these packages.

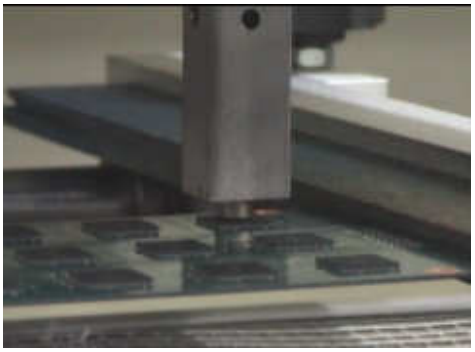
The rework process involves the following steps: “Component Removal”,” Site Redress”,” Solder Paste Application”, “Component Placement”, and “Component Attachment”

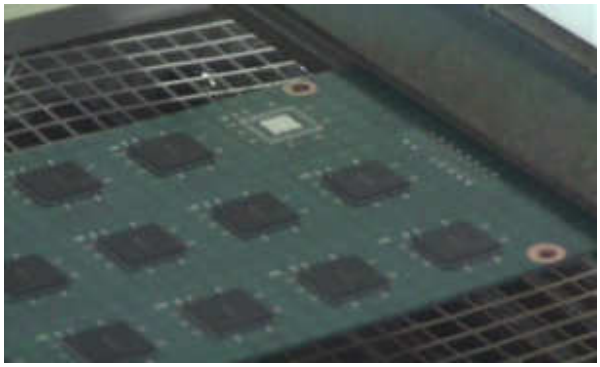
These steps are discussed in the following in more detail. Prior to any rework, it is strongly recommended that the PCB assembly be baked for at least 4 hours at 125^{o}C to remove any residual moisture from the assembly

6.1 Component Removal

The first step in removal of component is the reflow of solder joints attaching component to the board. Ideally the reflow profile for part removal should be the same as the one used for part attachment. However, the time above liquid can be reduced as long as the reflow is complete.

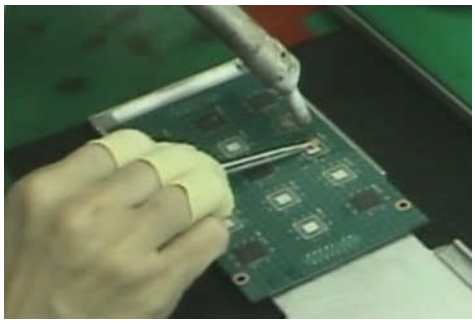
In the removal process, it is recommended using rework machine to do rework, it could get good rework quality, the heating profile setting could using same profile with mass production, the board should be heated from the bottom side using convective heaters and hot gas or air should be used on the top side of the component. Special nozzles should be used to direct the heating in the component area and heating of adjacent components should be minimized. Excessive airflow should also be avoided since this may cause aQFN to skew.

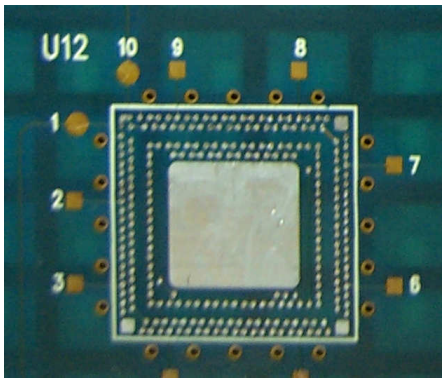




6.2 Site Redress

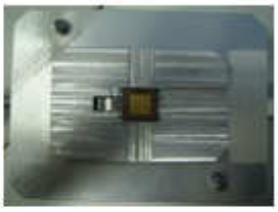
After the component has been removed, the site needs to be cleaned properly. The residual solder must been removed, the lands should be cleaned with a solvent. The solvent is usually specific to the type of paste used in the original assembly and paste manufacturer's recommendations should be followed.



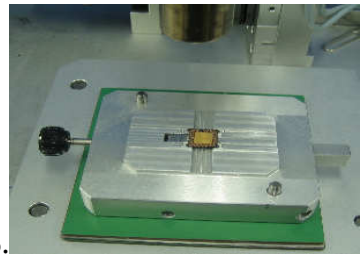


6.3 Solder Paste Printing and transferring to aQFN

As below picture showing, it needs a special rework stencil to transfer solder past to a new and good aQNF component, first put aQFN on fixure, then print solder paste on aQFN by stencil and heat it to make solder joint on aQFN leads.

1. 
2. 
3. 

4. 

5.  6. 

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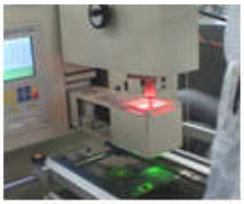
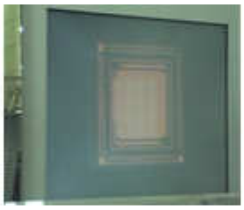
6.4 Component Placement

Before component placement, don't forget adding some flux both on aQFN component and PCB board, aQNF packages are expected to have superior self-centering ability due to their small mass and the placement of this package should be similar to that of QFNs. As the leads are on the underside of the package, split-beam optical system should be used to align the component on the motherboard. This will form an image of leads overlaid on the mating footprint and aid in proper alignment. Again, the alignment should be done at 50 to 100X magnification. The placement machine should have the capability of allowing fine adjustments in X, Y, and rotational axes.




6.5 Component Attachment

The reflow profile developed during original attachment or removal should be used to attach the new component. Since all reflow profile parameters have already been optimized, using the same profile will eliminate the need for thermocouple feedback and will reduce operator dependencies.

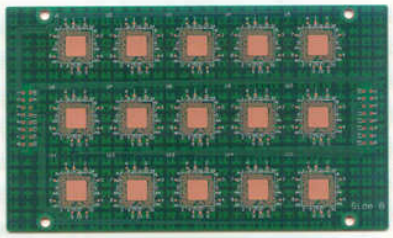
7.0 Board Level reliability Test (ref. JEDEC-22-B111)

The purpose of this study is for understanding the capability of board level reliability of aQFN .

I. Package profile

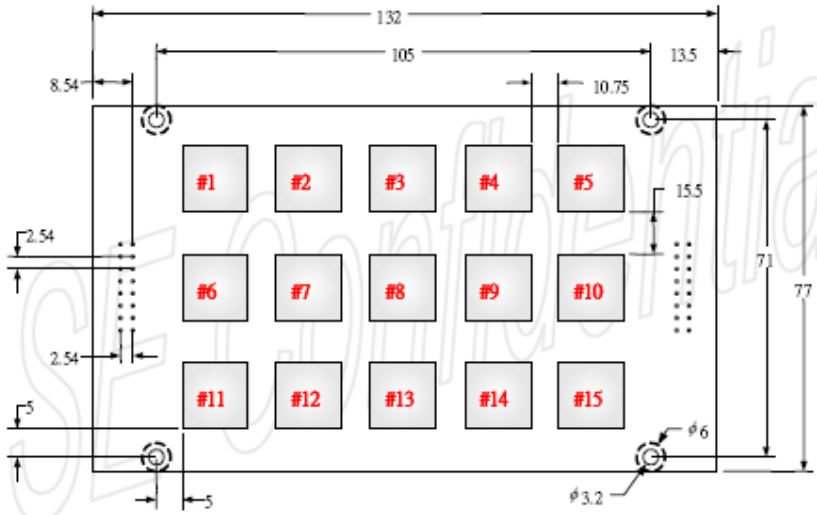
Item	Parameter	Value	Unit
Package information	Customer	ASE	
	Device name		
	Package type	aQFN	
	Package size	11.5x11.5	mm^2
	Lead count	261	L
	Die size	5941x5712	um^2
	Die thickness	6	mil
	Schedule	32YU1B	
	Epoxy type	EN-4900F	
	CPD	G700LA	
	CPD thickness	0.675	mm
	Wire bond material	Copper	
LF	Vendor	SUM	
	Thickness	0.13	mm
	Anchor lock	Yes	

➢Test vehicle

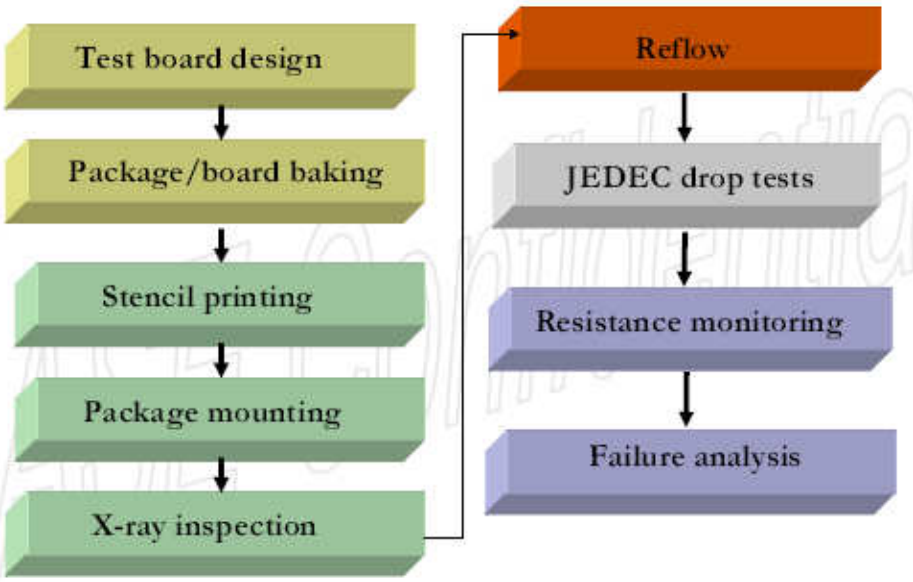


Vendor : Plotech
PCB drawing no. : 5600-91-A000-D102
Manufacturing date : 2010/ww01
Dimension (L x W): 132x77 mm^2
Thickness: 1.0 mm
Layer: 8 L
Pad : 0.27 mm /NSMD
Opening : 0.37 mm
Material: FR-4
Pitch: 0.47 mm
Solder paste type : SAC305
Solder paste model: M705-S101-S4
SMT : No via side
Surface finish : OSP
PCB design follow JESD22-B111

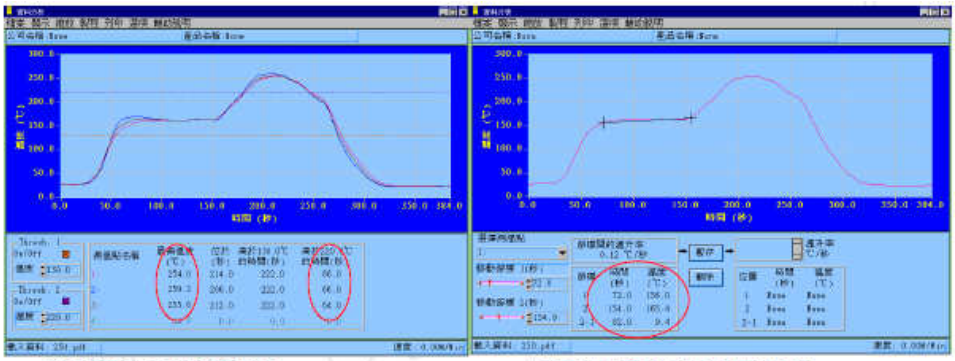
Board configuration



Experimental procedure



SMT profile for lead free



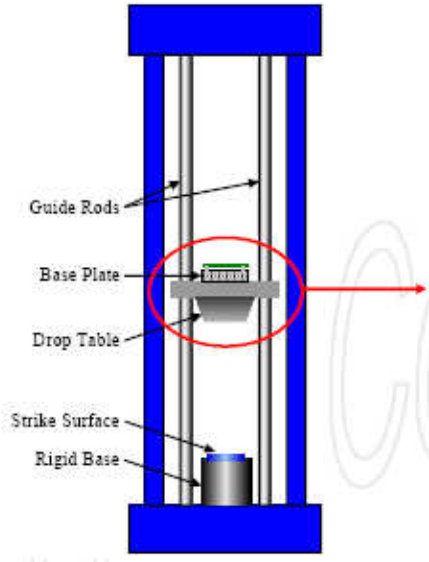
PROFILE CONDITION

- *BETWEEN 155 ~ 165℃ : 60 ~ 90 SEC.*
- *ABOVE 220 ℃: 60 ~ 90 SEC.*
- *PEAK TEMPERATURE : 250 ~ 255 ℃*

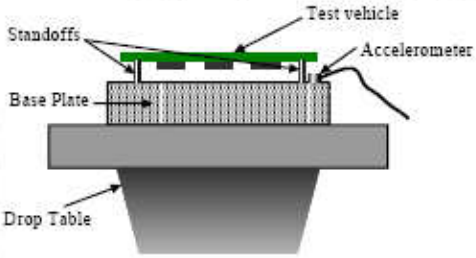
ACTUAL TRY-RUN RESULT

- *BETWEEN 155 ~ 165℃ : 82 SEC.*
- *ABOVE 220 ℃: 66 SEC.*
- *PEAK TEMPERATURE : 254 ~ 255℃*

Drop configuration



JEDEC drop test apparatus



Mounting scheme for PCB assembly

Test result

Cell No.		#1	#2	#3	#4	#5	#6	#7	#8	#9	#10	#11	#12	#13	#14	#15	Drop	First failure
20%	A	75	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	100	75
	B	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	ok	97	100	97

IV. Summary

JESD22-B111 board-level drop tests (condition B) are carried out, drop performance of ASE aQFN 11.5x11.5 261L, currently status:

1. All boards are passed 30 drops after performing repeatedly test.
2. From the investigation of dye penetration, it is observed that the main crack phenomenon of is pad peeling on test board side. Furthermore, from cross section result, the most crack is pad peeling on test board side

8.0 Reference Document

- 8.1 IPC-T-50 Terms and Definitions
- 8.2 IPC-SM-7351A or -782 Land Pattern Design
- 8.3 IPC-A-610 Assembly Acceptability
- 8.4 IPC-7711 Rework of Electronic Assemblies
- 8.5 JEDEC-020D MSL
- 8.6 JEDEC-033 MSL
- 8.7 JEDEC-22-B102 Solderability
- 8.8 JEDEC-22-B104 TCT Test
- 8.9 JEDEC-22-B111 Drop Test
- 8.10 JEDEC-22-B113 Bending Test
- 8.11 EIA/JESD-2 & -7 Thermal Performance Test