

nRF54L15 Specification update – 2024-09-03

Supply and GPIO voltage

This notice communicates a planned update to the product specification for nRF54L15. The update is an improvement of the supported power supply and GPIO voltage range.

Impacted products: nRF54L15-QFAA, nRF54L15-CAAA all revisions

Planned changes to nRF54L15 Objective Product Specification compared with v0.6:

- **nRF54L15 Feature List**
 - Update: “1.7 V to 3.6 V supply voltage with up to **3.6 V** I/O voltage”. Previous specification: “1.7 V to 3.6 V supply voltage with up to 2.6 V I/O voltage”
 - Update: “Up to 32 GPIOs at 1.7 V - **3.6 V**”. Previous specification: “Up to 32 GPIOs at 1.7 V - 2.6 V”
 - These updates are an improvement from previous specification where I/O voltage was limited to 2.6V
- **5.8 REGULATORS**
 - Normal voltage mode will have an increased input voltage range. The input voltage range for VDD shall be 1.7-3.6V
 - The on-chip LDO regulator VREGM is no longer required to support the supply range of 1.7-3.6V and will be removed from the power architecture.
 - Medium voltage mode will no longer be a supported voltage mode and will be removed from the Product Specification as it is no longer required.
- **10.1.3 QFN48 Pin Assignments**
 - Pin 48 currently named VDDM shall be renamed VDD.

Reason for change

Characterization of Engineering silicon has determined that the technology can support the increased VDD supply and GPIO voltage with no concerns regarding device reliability or lifetime.

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Supply and GPIO voltage - Implementation guidelines

Reference Design Update

An updated reference design is planned for nRF54L15-QFAA. The update will include power supply updates, and the RF matching network changes required for the nRF54L15 version Engineering B. In the interim, hardware designers are advised to connect VDDM pin to the same net as VDD pins.

Hardware Design Guidance for PCB designers

- **Supplying SoC through VDD pins – Normal voltage mode configuration.** If your existing design supplies in the range 1.7-2.6V no change is required to your design. For new designs, you have the flexibility to safely supply up to 3.6V to VDD. GPIO will be at the same voltage as the VDD supply.
- **Supplying SoC through VDDM pin – Medium voltage mode configuration.** Medium voltage mode configuration will be discontinued in the production version of nRF54L15, as it is no longer required to support the full supply range 1.7-3.6V. Designs must be updated to connect VDDM to VDD to prepare for the nRF54L15 production revision which will not support the VREGM regulator.

Guidance for use of existing hardware

For existing hardware designs including nRF54L15-PDK, the following guidance applies.

- If circuits connected to nRF54L15 can tolerate the voltage supplied to VDDM, it is possible to safely configure the VREGM regulator in bypass which will result in VDD=VDDM=GPIO HIGH. This option is not available in nRF Connect SDK today, it will shortly be available in the main development branch of nRF Connect SDK and future SDK releases will enable the bypass by default.
- If external circuits cannot tolerate above 2.6V, changes must be made to your design, the production version of nRF54L15 will remove VREGM functionality and VDD = GPIO voltage.

Support

You can already ask any questions regarding the nRF54L15 on DevZone with private tickets. We have established a dedicated Technical Support team for nRF54L15 to ensure that you have the best possible experience. Link: [DevZone](#)